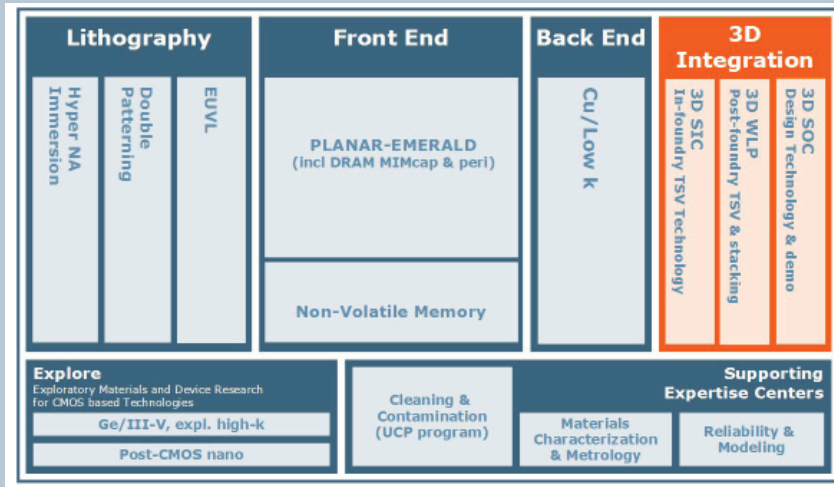


Back-End-of-Line 3D Integration

Positioning

This IIAP is part of IMEC's R&D platform towards sub-32nm CMOS:



Scope

The goal of the program is to concurrently explore the technology and design issues associated with several 3D application domains. The scope of the program is twofold:

- explore technology options and propose innovative solutions for the cost-effective realization of 3D interconnects at different levels of the wiring hierarchy: from the package level, down to the local on-chip interconnect levels;
- explore the design space and propose methodologies for critical design issues, enabling the effective use of 3D interconnection on the system level.

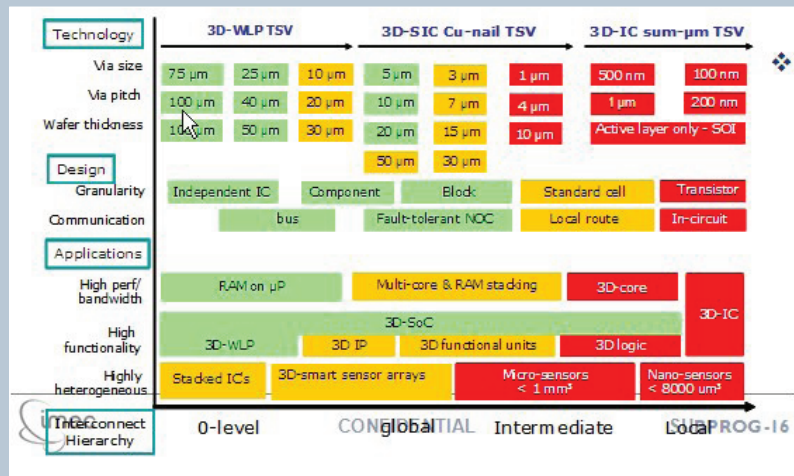
3D system integration explores the possibilities to interconnect active devices in different 2D planes. These interconnects can be considered at different levels of the wiring hierarchy, from the package, over the global to the local interconnect levels.

As 3D moves down in the interconnect hierarchy, the density of 3D interconnects increases exponentially, with different impact and constraints at the design and/or application level. The overall goal of the 3D system integration program is therefore to concurrently explore the technology and design issues associated with several 3D application domains.

In the program's roadmap, the 3D technology development will be driven by key system requirements (e.g. cost, testability, functionality and power). These requirements are translated in a top-down fashion into specs for the 3D technology development. Vice versa, 3D technology will be measured in Si and modeled for steering and fine-tuning the proposed design innovations. For this purpose, a design flow is put in place for bridging the gap between technology and design. The tight interaction between system design and technology and development will create the opportunity for exploiting the full potential of 3D technology in due time.



The following roadmap is driving the program:



Structure & Activities

The 3D integration program consists of tightly coupled sub-programs:

- 3D WLP: 'post-passivation' wafer-level-packaging integration. 3D interconnects are realized at the IC-bond-pad level, or 0-level packaging level.
- 3D SiC: 'Cu-nail' through-Si via technology integrated 'in-foundry' process (active program since 2006). 3D interconnects are realized at the global on-chip interconnect hierarchy level.
- 3D IC: wafer stacking for interconnects at the IC local interconnect level, requiring sub-micrometer through-Si via connections. This activity is positioned as long-term research. Exploratory activities through PhD topics will be reported in the existing program.
- 3D SoC: exploration of the impact of 3D SiC and 3D IC technologies on the system design of advanced systems.

Partners

1. IDMs;
2. semiconductor packaging companies;
3. fablite and fabless companies;
4. EDA houses;
5. equipment and material suppliers.

By combining expertise of the different players in the semiconductor value chain, partners at IMEC obtain key know-how and technology to optimally benefit from the potential of 3D integration. Supporting values are state-of-the-art facilities and a strong background in processing, packaging and system design.



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