**Product Brief**

**KEY FEATURES**

- **Outstanding Performance**
  - High throughput: 0.5GS/s and 1GS/s
  - INL/DNL below 0.1LSB
  - Small active area: 0.11mm\(^2\)
  - Low supply: from 1V down to 0.75V

- **Ultra Low Power**
  - 1.6mW for 1GS/s mode
  - 0.47mW for 0.5GS/s mode
  - Leakage below 1uW
  - Dynamic power consumption from DC to 1GS/s

- **Highly Integrated**
  - 16 channel time-interleaved
  - Low time skew signal/clock distribution circuits

- **Calibration Simple**
  - Gain/Time skew mismatch immune
  - Offset calibration method simple

**APPLICATIONS**

- IR UWB: ranging, localization.

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**PRODUCT SUMMARY**

**Description**

This ADC is a 16-channel time-interleaved 5-bit ADC for UWB radios. Each slice is asynchronous Successive Approximation Register (SAR) core.

Two relevant modes are supported: 1GS/s at 1V supply and 0.5GS/s at 0.75V supply. The ADC consumes 1.6mW and 0.47mW at the two modes, yielding 36 and 57 fJ/conversion-step FoM (Figure-of-Merit) respectively.

**Block Diagram**

This ADC is an 16-channel time-interleaved 5-bit asynchronous SAR ADC for UWB radios. It proposes 400aF unit capacitors, offset calibration, a self-resetting comparator and a distributed clock divider to optimize the performance. Only a simple calibration of the channel-offset is needed while the other error sources (Gain mismatch error, time-skew error, etc.) are minimized by intrinsic design. The offset calibration settings are loaded via the on-chip SPI registers. And the outputs of the 16 channels (16 × 5bits) are multiplexed on-chip into 4 channels outputs(4 × 5bits) to save pad numbers.

The offset calibration of the ADC is controlled by a digital SPI interface. There are 16 registers numbered 0 to 15. Register \(<n>\) is the ADC offset calibration for channel \(<n>\). Each register can tune the channel offset from -7\(\frac{1}{2}\) LSB to +7\(\frac{1}{2}\) LSB.

**INL/DNL**

After calibration, the measured INL/DNL are well below 0.1LSB.

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EVALUATION BOARDS

Spectrum at near-Nyquist tone

An on-chip crystal before calibration, the linearity is limited by offset mismatch. After calibration, the offset-spurs are reduced to -49.1 dB which is negligible for 5 bit accuracy. The figure also confirms that gain and time-skew errors are negligible in this design (-49.0 dB).

ENOB Versus input frequency

After calibration, an ENOB of 4.7 / 4.8 bit is achieved. Thus power efficiencies of 36 fJ and 57 fJ/conversion-step are achieved at 0.5 GS/s and 1 GS/s respectively.

For more information

Please visit [www.imec.be](http://www.imec.be) for more information about this and other products

About Imec

Imec performs world-leading research in nano-electronics. We leverage our scientific knowledge with the innovative power of our global partnerships in ICT, healthcare and energy. Our goal: creating innovative solutions that are relevant for the industry.

Imec’s research is 3 to 10 years ahead of the industry. We form a bridge between the fundamental research at universities and the technology development in the industry. Imec has a unique expertise in chip processing and system design, a strong IP portfolio, an ultramodern infrastructure, and an extensive network of partners. This makes us your premier partner to develop the technology of the future.

Imec is headquartered in Leuven, Belgium. We have additional R&D teams in The Netherlands (Holst Centre in Eindhoven), China, Taiwan, and India, and offices in Japan and the USA. Our staff of close to 2,000 people include more than 600 industrial residents and guest researchers. In 2011, imec’s revenue (P&L) was 300 million euro.

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Imec provides evaluation boards (EB) on request to prospective customers and partners interested in licensing imec’s radio designs and IP.

- **LUPUS EB**: allows complete evaluation of the ADC with the assistance of external FPGA board.

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<td>Power consumption (mW)</td>
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<td>Sample frequency (GS/s)</td>
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<td>ERBW (GHz)</td>
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<td>FoM (fJ/conversion.step)</td>
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<tr>
<td>Common mode voltage (V)</td>
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EVALUATION BOARDS

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