

# **Improving links between MANUFACTURING & SCIENCE**

*A framework for establishing  
a more productive  
industry/research link  
in support of the  
competitiveness  
of the  
European microelectronics  
manufacturing*

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## Table of Contents

Introduction .....	1
The “knowledge – manufacturing” gap .....	1
The “design” gap.....	3
Why now? .....	4
Different typologies/ domains in the industry/ research link .....	5
Scaling CMOS: the ‘classical’ microelectronics R&D .....	7
Additional functionalities: the Big Bang of microelectronics.....	13
The ‘Nano-world’ .....	18

## Executive Summary

A widening “knowledge-manufacturing” gap is observed in Europe as the request for scientific expertise from the microelectronics industry surpasses by far the ability of the European academia to provide. It is thus critical to propose a more productive link between industry and research in support of the competitiveness of the European microelectronics manufacturing.

The suggested schemes are different if we are considering the classical CMOS scaling, the addition of functionalities on a circuit or the introduction of nanotechnologies.

The **CMOS scaling** is a very special research field: it is resources and capital expenditure intensive (esp. with the transition to 300 mm wafers), while being extremely time critical. The issues are known along with the timetable (as sketched by the ITRS), most of the ideas exist, but often practical solutions have not materialized. The following recommendations are made:

- **Capitalize on the diversity of Europe** as long as the critical mass of expertise and funding exists, rather than trying to reach the perfect complementary between the different centers of expertise within Europe.
- **Select European Competence Clusters around few locations** (typ. Dresden, Grenoble and Leuven) where state-of-the-art 300 mm infrastructures are operated by major applied research Institutes (typ. CEA-Léti, Fraunhofer Gesellschaft and IMEC). Leverage the cost of these infrastructures through a close link with industrial sites (typ. Dresden and Grenoble) or by sharing the financial burden with non-European regions (typ. Leuven).
- **Complement these European Competence Clusters with networks of academia centers**, strongly linked with advanced industrial sites for manufacturing awareness. These academia centers with a critical mass of expertise, having acquired an international leadership through a constant focus on their field of expertise, should have an organized and funded access to the 300 mm infrastructures. They should have also the capacity to rely on small low-cost flexible additional clean-rooms or labs for value-added exploratory research.
- Capitalize on the excellent European education system and **support academia in making microelectronics industry more attractive**/ stimulating for young people.

**Adding new functionalities** in a System on a Chip leads the microelectronics research and industry to enter fields often new to them, not chartered by widely accepted roadmaps and where many other R&D and industrial actors may play a significant role. In this domain, where Europe may have a lead, esp. in the telecommunication and automotive markets, the following recommendations are made:

- **Promote teaching of interdisciplinary work.**
- **Promote interdisciplinary campuses:** the innovation ‘melting pot’ will be favored through the co-localization of education, SME’s and small R&D teams. In these ecosystems, the microelectronics industry may find the key competences for their differ-

entiation, as long as it supports the development of an independent (or even competing) expertise ground in Europe.

- **Balance the benefit of an exclusive R&D and the benefit of maximizing the information sharing** and the cooperation network for enhancing the creativity.
- The microelectronics industry should **use the major multidisciplinary R&D Institutes as vehicles** for understanding the new markets, getting access to a broad range of pre-existing knowledge and to make the ‘impedance-matching’ with the academia network.
- These major Institutes should **organize regular research-industry users’ topical meetings** within Europe to enhance the awareness of the European strongholds.

Europe entered early the **Nanoworld** with the European academia as a major player. Unfortunately, the rest of the world is taking over this leadership. In order to regain this leading position, the following recommendations are made:

- **Force early coordination in researches on materials, devices and system architecture of nano-objects**: the challenge of many novel nanotechnologies is less in producing isolated nano-devices than in implementing them in a manufacturable complex system.
- **Organize regular meetings between key researchers and industry senior managers** in order to present the critical assessment of the potentialities of ‘emerging’ technologies and to confront the optimistic views with the true manufacturing challenges.

## Introduction

Why do we have to pay renewed attention to the impact of scientific research on the development of microelectronics manufacturing? And why now?

The reason is that we are facing two new challenges:

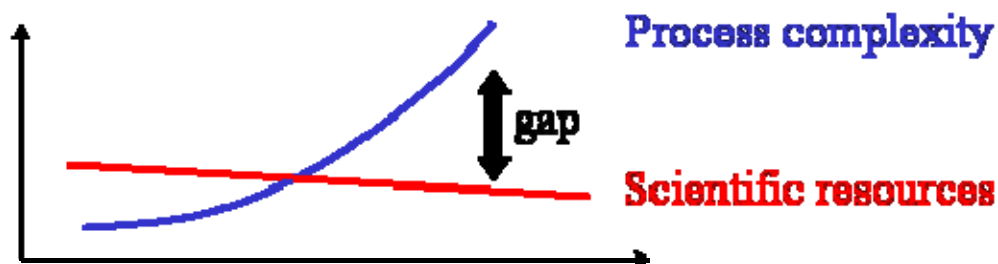
- the “knowledge-manufacturing” gap
- the “design” gap

### ***The “knowledge – manufacturing” gap***

The complexity of the manufacturing process is increasing exponentially: in order to maintain the doubling of device performance every 2 to 3 years, new materials, new process techniques and new device architectures are introduced with continuously increasing requirements with respect to yield, cost and quality.

In order to meet these challenges the semiconductor industry was forced to consolidate: R&D agreements between major players is common practice, few equipment and materials suppliers are left, R&D is mostly performed in pilot production lines. This R&D focuses on process integration and industrialization, usually at the expense of advanced R&D. Through this concentration the necessary critical mass for short term R&D can be obtained.

At the same time, the European academia partly moved away from the core microelectronics R&D, lacking more and more the dedicated human resources, motivated well-trained students and PhDs and adequate R&D infrastructures. The major European Clusters of Competence in Microelectronics<sup>1</sup> have made it their mission to fill that gap, but they in turn depend on thriving academia as their source of creativity and human resources. The diminishing resources of and contributions from academia then raises a severe and important question: how to encourage and enable academia to efficiently contribute to the advanced research in microelectronics, in spite of the obstacles, which make academic contributions somewhat difficult?



**Fig.1.** The “knowledge – manufacturing” gap arises from the growing discrepancy between the need for extensive research on the complex manufacturing processes and the decreasing scientific resources devoted to that field

<sup>1</sup> around CEA-LETI, the Fraunhofer Gesellschaft and IMEC

This gap might become dramatic.

The lack of adequate scientific resources may have severe consequences onto the European semiconductor industry: new processes and devices could be more and more poorly understood and controlled, breakthroughs may not be anticipated, the innovation could shift to other regions, esp. Asia/Pacific.

From the technical point of view, we are facing several challenges which will require huge amount of new skills:

- we are approaching technical limits of the classical CMOS: more R&D is needed esp. in modeling and physical understanding of the limits
- to overcome these limits, we need to explore new materials, new device architectures where many options are still open, the concepts have to be proven and the actual limitations assessed
- we are entering into the mesoscopic domain (in between the micro- and nano-world) where there are disruptive changes in device physics: materials can no longer be considered as homogeneous and not yet at the atomic level, quantum effects are more pronounced and 3D and interface/surface phenomena are prevalent.

### **Some key challenges of the semiconductor research**

*Being closer to the physical edge requires*

- better physical understanding of materials, processes, devices and characterization
- patterning at the nm-level: lithographic resolution/overlay/control/cost
- atomic layer handling
- accurate metrology and physical/chemical characterization of nm-sized structures

*Advanced materials and process innovation for pushing back the limits:*

- enhanced electrostatic control of the conductive channel and better isolation: SOI substrate, high-k insulating gate material, metal gate
- electrical conductivity limits: materials/substrates with enhanced mobility, saturation velocity, resistivity
- thermal conductivity: new heat dissipation techniques
- control the signal integrity: low-k materials, air gap for long-range interconnects, new substrates, shielding techniques
- new methods for reliability, failure analysis of the new materials and stacked structures
- accurate tool modeling
- advanced soft (bio)chemistry, self-assembled materials (SAM) for material deposition/ structuring

*Disruptive changes in device physics, esp.:*

- 3D phenomena
- prevalence of interfaces and surfaces vs. bulk behavior
- more pronounced quantum effects

**Some key challenges of the semiconductor research (foll.)**

*Dealing with the process complexity requires*

- reduction of process tolerances and/or development of fluctuation resistant architectures
- defect detection and characterization for failure prediction
- multilevel simulation tools (ab-initio and atomistic to continuum to device/ gate/ system/ service levels) for accurate predictive behavior at different scales

*Dealing with research fields outside the Si community for enhanced functionality:*

- magnetic material physics and devices
- non-Si active devices (III-V, carbon nanotubes, polymeric materials,...)
- MEMS
- biotechnology

*Enhancing the semiconductor research supply chain:*

- promote the education in technology
- ensure state-of-the-art R&D infrastructures
- promote coopeition (i.e. cooperation on some subjects along with competition between research teams for favoring the challenging and innovation spirit)

- we have to integrate some of the knowledge and results of other research fields (e.g. nanotechnologies, microsystems and, possibly, biotechnologies) in order to enhance the functionality of the resulting System on a Chip (SoC)

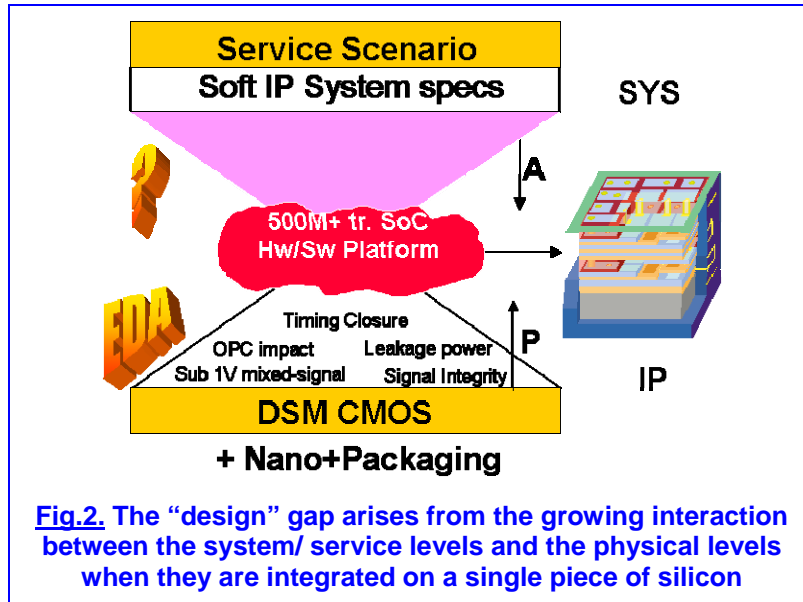
***The “design” gap***

The semiconductor industry is organized horizontally in order to be able to produce complex systems on a chip: well-defined system – design – technology interfaces were developed between each level (standards; libraries; design rules; etc.) in order to efficiently handle the design chain from specs to manufacturing. This contributed to the success of this industry in that experts could focus on their own field without caring too much about the impact on the other fields. These interactions can’t be anymore neglected (e.g. OPC, fluctuations, etc.) as they have a direct impact on the final yield and cost of the integrated devices.

Unfortunately the exponentially growing complexity of these interactions between the different levels results in a “design” gap which is widening without satisfactory solutions.

This “design” gap will restrict our ability to address key topics such as “Design for Manufacturability”, “Design for Yield”, “Design to Power”, accurate circuit modeling through realistic parameter extraction and simulation, concepts such as SoC’s and NoC’s (Network On Chip which might modify drastically the interconnect requirements), HW/SW security on the chip, a.s.o.

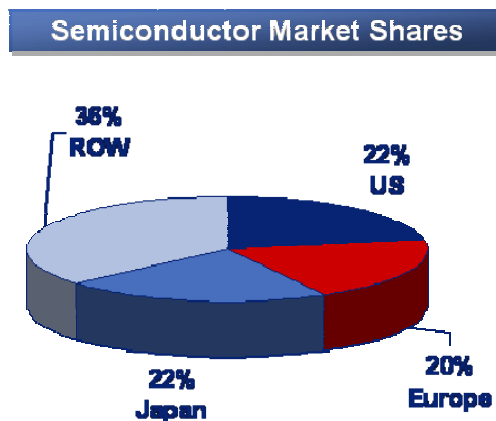
This new “design” gap adds to the more classical issue of the growing discrepancy between design productivity (expressed as number of gates designed per designer and per year) and the potential increase in integration density of the semiconductor technology.



Finally the integration of new functionalities will enhance the need of a better modeling and design flow for heterogeneous devices (sensors, actuators, etc.) where the modeling of non-electronic parameters will add complexity to the overall picture<sup>2</sup>.

**Why now?**

Europe is underrepresented in the worldwide semiconductor market and Europe is expected to loose market share in the semiconductor business to the benefit of the Asia-Pacific region, if no strong action is undertaken.



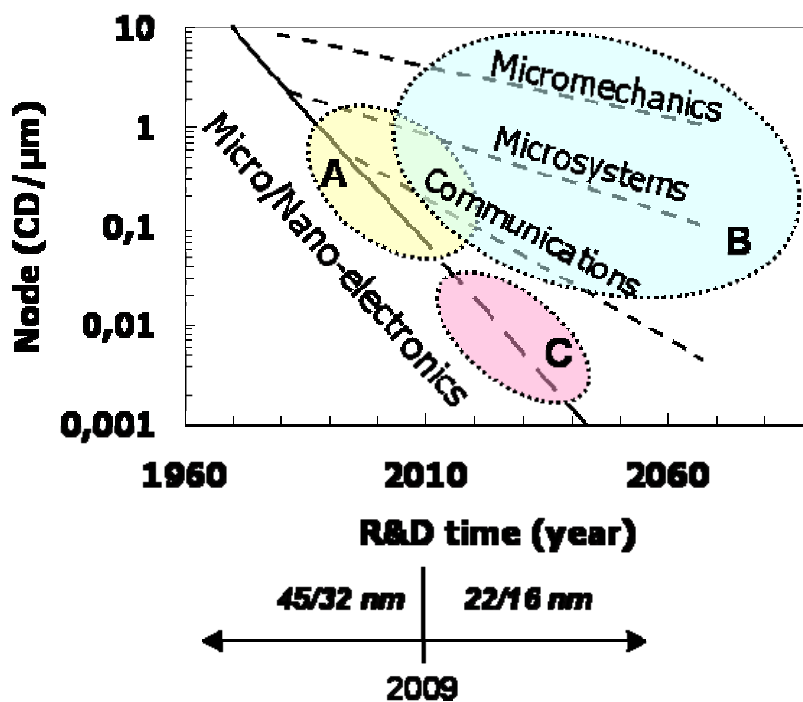
**Fig.3.** Europe is underrepresented in the worldwide semiconductor market

<sup>2</sup> See for more details the previous report of the MEDEA+ Scientific Committee on “Heterogeneity on Si or in a Package for Future System Innovation” (2003)

Ensuring a more productive industry/ research link to enhance innovation is thus key to support the future competitiveness of the European microelectronics manufacturing and to keep jobs on value-added technologies in Europe.

**Different typologies/ domains in the industry/ research link**

The performance and competitiveness of the semiconductor industry is usually benchmarked through the so-called ‘Moore’s Law’, which assumes that the reduction of the physical dimensions in an IC will bring at the same time higher speed and integration density, lower cost per function, better reliability and expanded markets and revenues.



**Fig. 4.** The research fields allowing progress in semiconductor manufacturing can be divided in 3 major blocks.  
**A.** the scaling of CMOS along the ITRS guidelines  
**B.** the added functionalities which can be integrated  
**C.** the nanotechnologies which can provide breakthroughs and enhancements in the present semiconductor technologies

Unfortunately this 1-dimensional picture becomes less and less accurate. We may see in the future different domains where the progress will follow different lines (s. **Fig. 4**):

- A.** Classical **CMOS scaling** will still continue for the next decade despite the growing difficulties in introducing new technologies at the same pace and at an affordable cost. R&D teams interacting with the semiconductor industry need to adapt to the growing access cost to state-of-the-art 300 mm infrastructures and equipments for performing time-driven research on more and more demanding materials and devices

- B.** All devices which are integrated in order to enhance the overall functionality of a System on a Chip do not scale that easy (or even do not scale at all). At the same time the growing diversity of the **added functions** and devices lead to introduce fields new to the Si community where many other R&D and industrial actors may play a significant role. This domain is sometimes called the '**Big Bang of microelectronics**'
- C.** Finally when entering the sub-10nm field, often dubbed as 'Nanotechnology', 'Nanoelectronics' or '**Nano-World**', new perspectives are offered through radically new physical behavior, function and devices, covering an extremely wide technical field. The key point is to sort out among the results and hypes of research teams which ones would be usefully introduced in the microelectronics field.

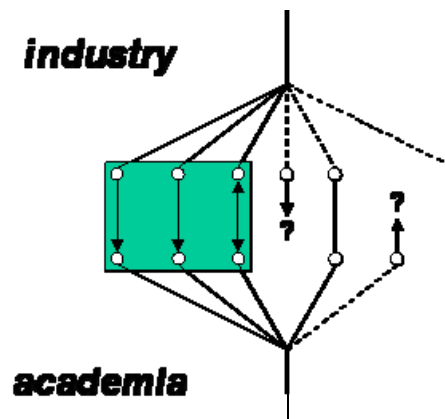
This report will thus analyze the different pattern of these three different domains and suggest some guidelines for a more productive industry/ research link in support of the competitiveness of the European microelectronics manufacturing industry.

## Scaling CMOS: the ‘classical’ microelectronics R&D

The R&D for scaling the CMOS technology is a very special research field: it is resources and capital expenditure (capex) intensive, while being extremely time critical. The issues are known along with the timetable (as sketched by the ITRS), most of the ideas exist, but often practical solutions have not materialized.

The drivers of the progress in microelectronics are the costs per function (obtained through shrink, yield and line utilization and new functionalities), the overall performance in power consumption – density – speed (at the system level) and the possibility to reuse the technology for more than one technology node. In future ESH (environment, safety and health) aspects will play an increasing role along with the social acceptability of the applications.

In microelectronics R&D, most of the short-to-medium term research is driven by industrial needs and issues. R&D teams interacting with the semiconductor industry should adapt to the time pressure and the market competitiveness which is at stake, along with the growing cost of performing this type of research. Suitable ways of cooperation have to be found to deal with less capex intensive topics partly at the R&D sites, while working on the capex intensive ones in joint environments.



**Fig.5. In microelectronics R&D (i.e. the ITRS scaling approach), most of the research is driven by industrial needs and issues. Items not known from the industry or the academia are unlikely**

Cooperation between academia and the semiconductor industry involves a number of different issues:

- the academic teams are spread all over Europe and a clear mapping of the existing expertise doesn't exist. This point has also been identified in connection with the current Framework program of the EC.
- as we are approaching the phase of process integration the cost of R&D is growing beyond the financial capacity of most of the R&D teams. This requires close cooperation between these teams and industry in the path from precompetitive research to integration; hence this can only take place at a few locations.
- manufacturing cost awareness and process complexity awareness are often not the key focus of academic teams. This means that research results which could be excellent,

e.g. in performance, may be problematic with respect to a potential introduction in manufacturing

- the need of a timely outcome of the research program leads the semiconductor industry to request the research teams to commit to time schedules which may be inconsistent with the search for real innovation in upstream research
- IP is a difficult matter, leading to long discussions on the ownership, the licensing and sublicensing rights, fees or exclusivity. The difficulty arises from the fact that academia and research institutes are often judged on one of these specific items or depend on them to partly fund their R&D (e.g. royalties); on the other hand the industrial partners use IP not as performance indicator, but as part of their overall strategy for increased competitiveness on the market. As such it takes time to reconcile the two positions.
- in most cases, academic R&D is sharing resources with its teaching commitments, whose goal may be conflicting with the short term requirement for dedicated resources

Academic R&D suffers of an image of scattered competence and a lack of clear focus. In order to promote enhanced efficiency:

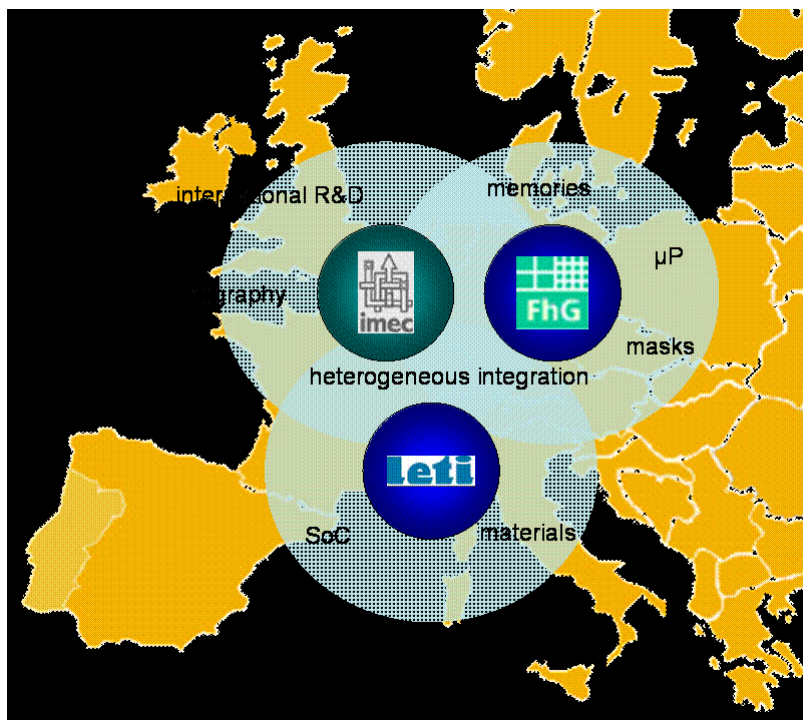
- the research institutions should encourage focused actions and teams with a critical mass, while the present situation of parallel activities with sub-critical resources performed all over Europe has to be avoided.
- on the other hand, the myth of the perfect complementarity between the different centers should not be pursued by the public authorities and the industry as long as the critical mass of expertise and funding exists: this goal of an absolute complementarity is probably difficult to achieve and can be counterproductive if it results in a single-minded research without any stimulating competition between few expertise centers
- the promotion of these focus centers should be well accepted and publicized by all the players in the semiconductor field
- the programs and funding should provide continuity in the research direction. Too often the research themes follow hypes, bringing too many teams competing in a single fashionable area. It should be stressed that industry shares its part of responsibilities as industrial requirements frequently change over time. It does mean that the scope of research must not be too narrowly limited, otherwise the risk increases that on a long-term run the necessary developments will not be made or not in time.

The cost issue for advanced R&D is a key limiting factor:

- the investment in state-of-the-art equipment and infrastructure for experimental work should be restricted to a limited number of research centers in order to achieve the needed economy of scale for the high capex part of the microelectronics R&D. The multiplication of sub-standard clean-rooms in the academia is a waste of money. On the other hand, R&D low cost clean-rooms may provide a substantial added value. Their flexibility, not limited by current production requirements, must be exploited to provide a better link between industry and R&D teams
- this cost is not restricted to capex, but also running cost should be taken into account in order to maintain this state-of-the-art infrastructure with a high efficiency
- in order to ensure the manufacturing awareness in the development of new technologies, a clustering of such research centers with advanced industrial sites is mandatory.

- the cost of the 300 mm R&D may be leveraged through a close link of such research centers with advanced industrial sites: the industrial infrastructure may ensure a higher speed of processing and an economy of scale (the “lab/fab” concept)
- another way to leverage this cost is to bring non-European partners to participate in cooperative programs in Europe: this may at the same time reinforce a leading role of Europe in the ITRS scaling
- these research centers have to be accessible to the academic teams in order to study state-of-the-art technologies. Only for the most exploratory research on new materials and techniques, low cost research equipment in low quality clean rooms (or even standard labs) should be accepted.
- these European competence clusters may aggregate distributed additional competence throughout Europe and thus achieve the critical mass of expertise. Furthermore it could bring more efficiency for very long term research, beyond the technology generation developed in applied research institutes.

**At the present time, three European competence clusters are in position to handle the high capex part of the academic research. These consist of R&D sites cooperating with industrial production sites, either in close proximity or with a well-established international cooperation scheme.**



**Fig.6. At the present time three European competence clusters being globally active players have the potential to attract capex intensive microelectronics R&D teams**

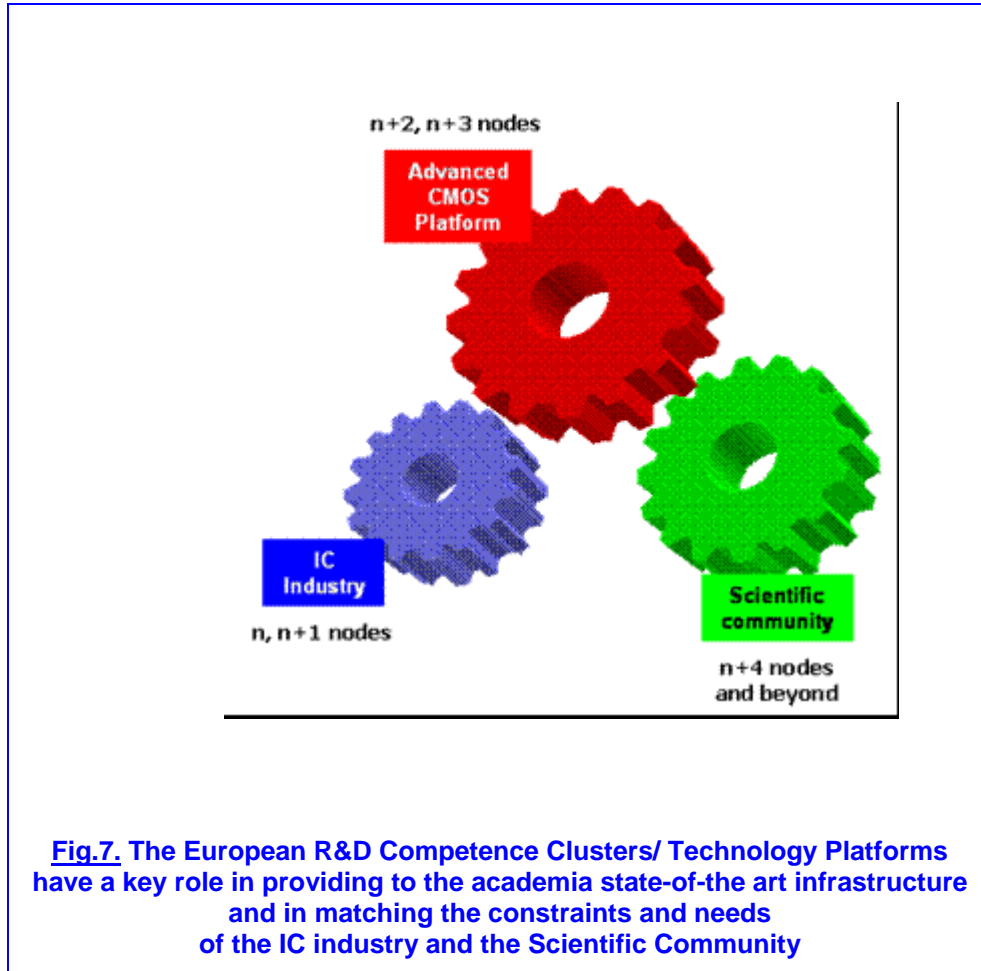
The academic world can have a substantial contribution to the progress of the microelectronics. The academia is the main source of scientific expertise which can be applied to microelectronics; as such it can contribute:

- in providing thorough understanding and precise characterization of the materials, processes and devices under development in a way the industry – and to some extent also the applied R&D institutes – can't provide
- in providing early models of the technologies under development
- in screening innovative concepts and materials in parallel before starting the costly applied research work. Academia is especially well suited for this early screening work due to its openness to related fields and the variety of competence in the labs
- in participating in R&D programs, having part of their teams assigned or working in the few European competence clusters which have the adequate infrastructure: through these assignments, a better awareness of the manufacturing issues will be developed, focusing the academic R&D on more immediate or pressing needs
- in bringing in their unique expertise in task forces on production issues: in order for that to be effective, direct links between the research teams and the industrial development teams should exist from past cooperation and/or this unique expertise should be made visible to the industry.

Expressed in a more general way, academia may provide the stimulating environment and the variety of ideas needed for advanced long term research which are often lacking in the short term oriented applied/ industrial R&D. For promoting this potential benefit, industry and applied research institutes should support the funding of academic projects , despite the fact that a significant part of the funding capacity in Europe has to be directed towards the more costly short-term applied developments.

Added to this technical contribution, academia has a unique role in making microelectronics industry more attractive/ stimulating to young engineers and in training excellence. One could think of launching a microelectronics attractiveness program, e.g. through an aggressive Public-Authorities supported PhD and post doc program, using the MEDEA label as a promotion tool worldwide; through MEDEA Research awards, etc..

In summary, the European R&D Competence Clusters have a key role in providing the academia state-of-the art infrastructure, in making the 'impedance matching'/ translation between the constraints and needs of the manufacturing and the academia and in helping build the right direct links between the expertise of academic teams and the industry.



### **Some key opportunities and challenges for Europe in the CMOS scaling**

*It is not the purpose of this report to duplicate the ITRS roadmap. The listed items are more to underline where Europe has particular strengths and in which fields urgent actions are needed in order to ‘stay in the race’.*

#### *Opportunities*

- capitalize on the multicultural nature of Europe for promoting a variety of ideas
- capitalize on the excellent education system in Europe
- capitalize on the few applied institutes active on 300 mm R&D in Europe (CEA/Léti, Fraunhofer Institutes and IMEC)
- strengthen the few technology strongholds of Europe (lithography, simulation, compact modeling,...)

#### *Challenges*

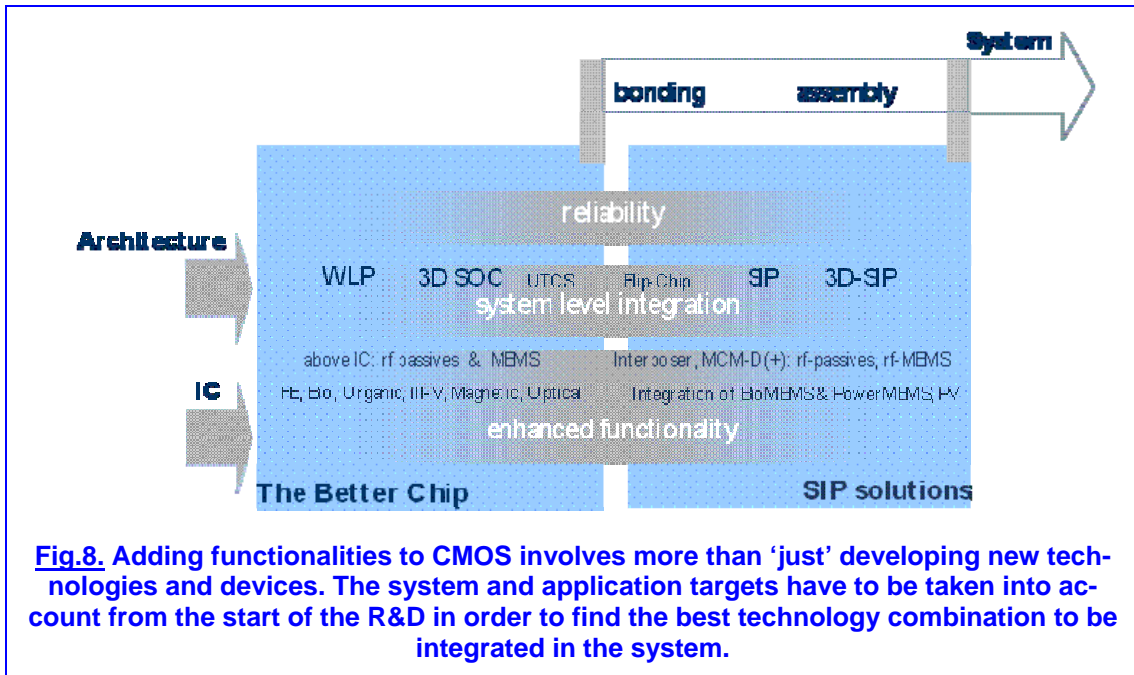
- develop European Competence Clusters with the right infrastructure and critical mass in strong relationship with the regions of advanced microelectronics industry (esp. Dresden and Grenoble)
- provide adequate support for European Competence Clusters which create European leverage through worldwide partnerships
- establish synergies between these Competence Clusters
- make microelectronics industry attractive for (young) talents

### Additional functionalities: the Big Bang of microelectronics

Adding new devices and new functionalities in a System on a Chip leads the microelectronics research and industry to enter fields often new to them where many other R&D and industrial actors may play a significant role.

These ‘new’ widely diverging fields involve other cultures, other working and business patterns which may be troubling for the microelectronics people. As an example, in strong contrast with the CMOS field, there is no (or too many) roadmap(s) sketching the future of added functionalities on Si: this is due primarily to the strong interlinking between the technology and the applications.

Finally the differentiation through additional functionalities is a key competitive advantage of the European microelectronics industry, leading it to be reluctant to share openly the knowledge and R&D. Scaled CMOS is becoming a commodity whose mastering is still needed to design competitive products, but which does not create in itself a key success factor on the market place.



The main characteristic of this domain is the broad spectrum of knowledge needed to add the right functionality to the scaled CMOS. As examples of this diversity:

<i>Integrating more functionality on Si</i>		
	Interfacing with the analogue world	switch analog circuitry to digital concepts
	Communications	SiGe-BiCMOS in line with CMOS logic scaling (as III-V contender)
		rf CMOS
		optical interconnects and integrated photonics
		integrated passives (e.g. RLC, resonators, mechanical filters,...), ferromagnetic and ferroelectric materials, rf switches)
	Microsystems	MEMS (batch fabricated)

	Energy management	smart power
		power-optimized design methodology
		integrated $\mu$ fuel cells and supercapacitors
	Integrating in a package	packaging (e.g. SiP, WLP, WLCSP, 3D integration)
		microhybrids (e.g. III-V on Si, multi-sensor systems)

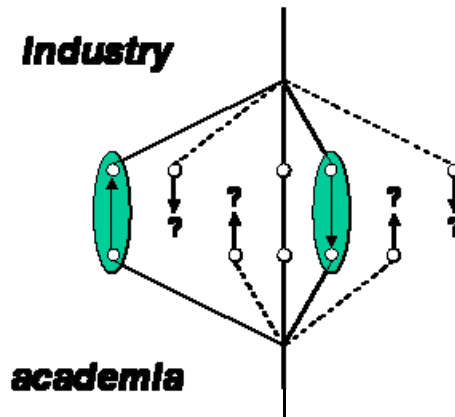
<i>Creation of derivative technologies</i>		
	Communications	unobtrusive radio (e.g. 'smart dust', 'ambient intelligence', 'pico radio')
		wireless sensor networks
		wearable electronics
	Microsystems	chemical lab on-a-chip (e.g. microfluidics)
	Nanotechnologies	nanocomponents in SoC's
	Biotechnologies	biomimetics

In this domain, a more productive manufacturing/ research link should allow the industry to have a timely access to a broad range of pre-existing knowledge developed outside the semiconductor industry and to prove that the concept is applicable in or above an IC and brings a competitive advantage. The industry needs highly skilled people in diversified fields, used to the interdisciplinary work and to a technology – system codesign-type of research. Due to the strategic impact of the outcome of the research, bilateral cooperation is preferred whenever feasible.

Academia can provide a useful manpower intensive work for early investigation of new concepts in an interdisciplinary environment: in that sense a multidisciplinary campus gathering a broad range of expertise is a key differentiating factor. One should have in mind that 10-15 years are needed to introduce a new material and that only academia can afford cross-disciplinary materials research on the long range. This work of trial & error approach of integrating different technologies has to be supported by a thorough scientific understanding of the results in order to refine better approaches and predict enhanced results in a more robust production environment using better equipments and infrastructure.

What is more specific to this field compared to the classical CMOS microelectronics – where the entry ticket is very high – is the possibility to rely also on a wealth of small and medium sized enterprises whose expertise develops outside the microelectronics field and may be of

great help for integrating new techniques on a CMOS wafer. The diversification of this industrial ground should be preserved and favoured.



**Fig.9.** In the more diversified fields of adding functionalities to CMOS, part of the research is done in different places and outside the microelectronics industry. The challenge is to better connect the different players of this R&D in order to induce a more efficient cross-fertilization.

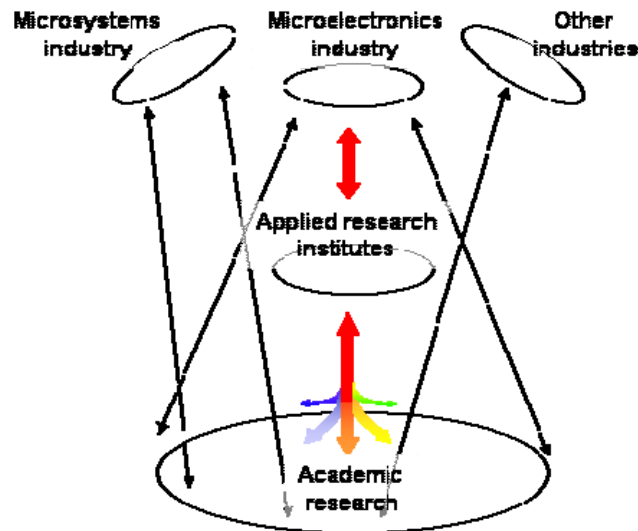
In order to take the maximum benefit of this situation, many paths are open:

- the major R&D Institutes still have an important role in terms of ‘impedance matching’, especially if their interdisciplinary character is strong: besides their internal expertise and the role of go-between they can play, they have also a first-hand knowledge of other business models which may be disturbing for people used to the microelectronics culture (e.g. in biotechnology, a single patent may prevent the entry in a market without any chance for a cross-licensing agreement)
- as the technology infrastructure is less critical for early assessment of these diversified technologies, some direct links between academia and industry are more likely and wishful in order to avoid the overhead associated with intermediate structures
- SME’s are important players which should be strongly supported for developing the right product/ application expertise ground in Europe
- in order to link all these actors, regular research – industry – users topical meetings should be organized beside the more classical formal conferences. The benefits of this networking actions are numerous:
  - it permits early identification of best in class solutions among the competing research approaches
  - it allows informal contacts between experts, contributing to avoid deadlocks (that was actually one of the great benefits of the early ESPRIT projects)
  - in some limited cases it allows direct know how transfers

On the other hand it may have some issues:

- decreasing competition and thus a lower creation of new ideas may result from the knowledge of competing researches
- efficient information exchange can be prevented by the sensitive character of the research (ownership of the results, know-how transfer to competitors, etc.)

In summary, trade-off has to be made between the benefit of an exclusive R&D (with a competitive advantage in preventing the research team to interact with competitors) and the benefit of maximizing the R&D diversity within the research teams in order to favor innovation in Europe.



**Fig.10.** The efficiency of the research activities in integrated functionalities in CMOS rely on the preservation of a rich network of industrial and academic teams taking care of the sensitive nature of the work. Applied research institutes may play a role in the animation of this network.

### **Some key opportunities and challenges for Europe in the field of added functionalities**

*The listed items underline where Europe has particular strengths and in which fields urgent actions are needed.*

#### *Opportunities*

- Europe has a strong background in system/ application oriented technological R&D
- Europe has a fertile ground through SME's for diversified integrable technologies
- Europe has some major interdisciplinary research institutes

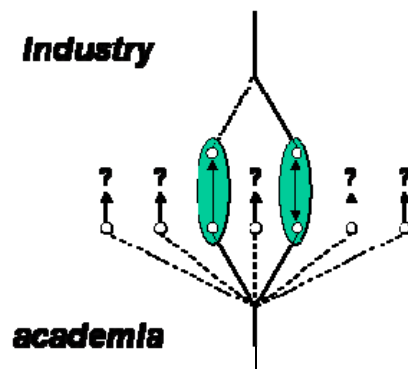
#### *Challenges*

- teach and favor interdisciplinary work and establish campuses that induce this kind of work
- adapt to other business models and cultures
- find the right trade-off between information sharing for enhancing the creativity and confidentiality in the sensitive research activities.

## The 'Nano-world'

Using potentially radically new physical behavior, function and devices as expected in the sub-10 nm regime, new perspectives are offered for implementing complex functions in an integrated circuit. Europe was well positioned in promoting nanoelectronics research<sup>3</sup>, but the rest of the world (esp. the US and the Asia/Pacific region) is taking over the leadership<sup>4</sup>.

This field is usually far away from the concerns of the present manufacturing lines and clearly academia is in the forefront of this research activity. However a better interaction between these two worlds could be beneficial in order to bring together the constraints of the integration and manufacturing of extremely complex systems and the potential benefits of the proposed approaches. Through this synergy which is more effective in the US, a really competitive research could emerge putting Europe in a good position for a realistic introduction of the nanotechnologies into complex microelectronic systems.



**Fig.11. The introduction of successful concepts of the 'Nano-world' into complex microelectronic systems will be mostly driven by the academia. A stronger interaction with the industry may benefit both sides.**

<sup>3</sup> the European Commission promoted an early roadmapping work on nanoelectronics within the MEL-ARI Initiative (s. Technology Roadmap For Nanoelectronics - Edition 1999 at <http://www.cordis.lu/esprit/src/melna-rm.htm>) which is cited even in the US.

<sup>4</sup> the section on the 'Emerging Research Devices' in the latest version of the ITRS is an interesting attempt to sort out many options for the future of microelectronics (s. <http://public.itrs.net/Files/2003ITRS/Home2003.htm>)

A clear issue is how to sort out between hypes, early announcements and true breakthroughs (see excerpt below).

### Hypes, fashion and failure are not new in research

*"Investigation of adventurous new technological approaches is a high risk enterprise. Most attempts to depart seriously from advancement of the currently established technology are likely to fail. New approaches need a supportive environment to have a chance. It is my contention that we not only provide this, but go too far and discourage critical assessment. It is the advocates who organize the conferences and the special issues of journals. The critic is likely to be left uncited. Those who are employed in the prevailing main line approach are, in any case, likely to just shrug in skepticism. They will hesitate to invest the time needed for a detailed technical assessment of a possibility they consider unlikely. They know that the advocates of a new approach have presented an optimistic vision and have compared that to what the prevailing approach can supply to the customer right now. The semi-popular journals, in their evaluations, can draw on an easier audience for the discussion of exciting novelties than for critical evaluations.*

*[...A specific proposal for logic implementation] attracted considerable and favorable attention [...]. By now, it has become clear that the pessimists were right; the proposals are almost forgotten. None of the enthusiasts have admitted a mistake. We can understand that on the part of the key protagonists, who can tell themselves that if only this or that had gone differently, they would have been successful. But it is not as easy to excuse the supposedly more objective scientific journalists.*

*[...] In the early stages of a technology the proponents have many incentives to publish, but we do not give awards for the best technical obituary of the year. And who is left to cite the paper that tells us that there is no longer any promise in the field? Will a university department be willing to consider such an obituary as a major reason for promotion to tenure, despite the fact that it cannot lead to grants?*

*[...] We do not, in the long run, build effective public support for science and technology by promising more than we can deliver. An occasional balanced view [...] does appear, but it is all too rare."*

*From Rolf Landauer, *Need for Critical Assessment* in IEEE Trans. Electron Devices, vol.43, no.10, pp.1637-1639, October 1996*

The way this adjustment between announcements and realistic expectation will be managed is key for the credibility of the whole domain:

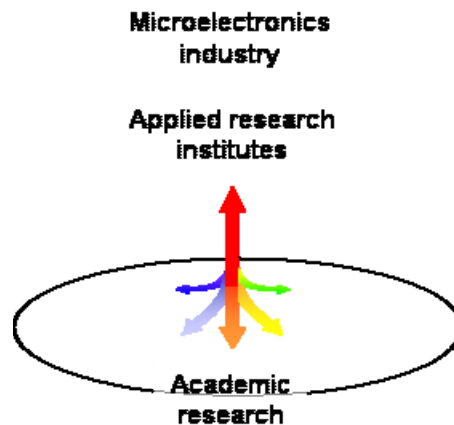
- hypes are counterproductive and do not serve the academia: they are often the result of an excessive extrapolation of only one parameter of a given device without taking care of the way (or even knowing the constraints of how) it could be realistically integrated in a complex system<sup>5</sup>
- on the other hand balanced views in less technical journals and books may help the executive bodies to focus on few promising options

<sup>5</sup> as a classical example, SETs were presented as transistors achieving an extremely high integration density because the 'active' part (i.e. the quantum dot) is in the nm range. On the one hand this very high integration density was never experimentally proven (published SETs are usually bigger than state-of-the-art MOS transistors). On the other hand the low gain of these transistors (if any) prevents their extended use in complex systems.

- through their expertise and network, academics monitor (and are source of) international progress:
  - environmental scan – who’s active in what? – is important in this multi-disciplinary field
  - ‘sniffing’ – identify embryonic/emerging opportunities & breakthroughs may help to early identification of promising solutions<sup>6</sup>

Some practical actions can help to enhance the research and industry synergy in nanoelectronics:

- promotion of multi-disciplinary campuses, research networks, open forums, workshops,...
- organization of a permanent innovation market place where application oriented and research people can do research together: a yearly presentation of the critical assessment of the progress on ‘emerging’ technologies could be organized to the industry leaders in order to reinforce the industry awareness of potential breakthroughs and to challenge the optimistic view of some researchers



**Fig.12. The efficiency of the research activities in nanotechnologies will result from the interaction mechanism between academia and applied research which will confront the expected performance of the new concepts with the expected progress in standard CMOS systems. This will allow reducing the number of options which will realistically be integrated in complex microelectronic systems.**

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<sup>6</sup> Such kind of activity exists in Minatec (Grenoble): the ‘Observatoire des Micro et Nanotechnologies’ publishes 5 times a year to its members a critical assessment of the published data in different fields like ‘Nanotechnologies’ and ‘Molecular Electronics’. This assessment is performed by a group of experts from academia and applied research institutes.

## Some promising fields for integrating nanotechnologies in complex microelectronic functional systems

### *Self-assembled structures*

- structuration ('self-organization') for preferred localization
- surface functionalization (molecular recognition)

### *Technology at the atomic level*

- single atom/ layer manipulation
- deterministic dopant placement ('self-organization', superstructures,...)
- advanced physical and characterization

### *Material engineering*

- nanostructured 'artificial' materials
- predictive simulation and modeling & computational material science

### *Carbon nanotubes*

- control of growth and properties (localization, diameter, chirality,...)

### *New memory concepts*

- 2<sup>nd</sup> and 3<sup>rd</sup> generation of MRAM
- Phase Change Memories (PCM)
- Nanocrystal Memories
- SONOS Memories
- other universal memories?

### *Architecture of complex systems*

- defect/extrinsic-resistant architectures
- fluctuation/intrinsic-resistant architectures
- functional to physical implementation

### *Quantum devices*

- spin electronics
- nano-dots
- hybrid quantum electronics

[quantum computing, if successful, is further away in the future]

**Some key opportunities and challenges for Europe in the 'Nano-world'**

*It is not the purpose of this report to duplicate neither the European Nanoelectronics roadmap or the Emerging Research Devices section of the ITRS. The listed items are more to underline where Europe has particular strengths and in which fields actions are required.*

*Opportunities*

- multicultural nature of Europe
- early European programs and roadmaps in nanoelectronics (MEL-ARI,...)

*Challenges*

- force early synergy and collaboration between material research, device research and system/ architecture research in nanoelectronics; for many novel materials, the challenge is no longer in producing the material (e.g. CNTs) but in implementing it in a device or a circuit
- promote balanced views of potential progress in nanotechnology