HETEROGENEITY ON SI
or
IN A PACKAGE
for
FUTURE SYSTEM INNOVATION

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EXECUTIVE SUMMARY

In the coming decade silicon devices will be divided into two main categories:

(1) bit rate performance driven digital ICs, following Moore's law on the ITRS roadmap, for which the US area is dominant

and

(2) mixed signal heterogeneous devices driven by cost and also other requirements such as low energy dissipation and integration of various technologies, where Europe may have a strong leadership. This category of devices follows a more diversified roadmap where the minimal dimension of the transistor is only one of the key parameters of the technology along with mixed-mode or RF components, embedded MEMS and bio-functions. For this type of system, **heterogeneity on silicon or in a package** is the main feature for system integration.

For the sake of simplicity, this report focuses on silicon technologies*, **excluding optical devices and systems**, as well as **flexible electronics** (e.g. on plastics)*. In the same way, harsh environments requiring dedicated technologies are not specifically discussed. It should also be stressed that **embedded software** is not detailed in this document, though it contributes to a large extent to the final cost of the system.

As an outcome of this study, the following recommendations are made with respect to the R&D efforts on heterogeneous systems to be pursued in the next decade:

1) **promote a holistic approach to the design of systems that have a high degree of heterogeneity.** This requires a new collaborative and multi-disciplinary approach to system level design and technology research driven by well-chosen long term focused application domains. Success in this area will depend on our ability to organize **collaborative research and education projects**, understanding each other's terminology and way of thinking over all levels of abstraction, merging presently unconnected domains like advanced software techniques to molecular electronics. The best formula is probably the creation of **Focus Centres of Excellence** of sufficient critical mass to support multidimensional teams to create demonstrator designs showing the feasibility and cost issues of design methodologies in a given process technology. At the same time such centres should be networked with the scientific community and results should be available for **dissemination** to the system design community.

2) **digital design challenges for heterogeneous systems** are important in terms of low-power computational efficiency. There is a need for advanced research in design methodologies for **ultra-low power** multiprocessor architectures of **programmable, memory dominated platform**. This translates in efficient ways to partition between hardwired, reconfigurable and programmable parts (**service/ architecture/ compiler co-design**), in **spatial / temporal localization of the data production and consumption** with special attention to design methods for low power memory

hierarchies and localizations, in **leakage reduction techniques** and in optimization between **on-chip and inter-chip networking**

3) **mixed signal design development** will be a key part of the heterogeneous system design, where architectures will compensate for analog precision by more **digital techniques** and by using more accurate **mixed modeling and simulation techniques**

4) **rf design** needs major improvements in accurate **macro-modeling** of the channel, verification and simulation **environment**, **digital compensation** of non-idealities, efficient model and simulation of the **signal integrity** (e.g. substrate noise)

5) **system package design** will require major breakthroughs in a multi-scale **co-design of chip and package** in order to optimize the overall size, performance and cost of the system. It includes an efficient **partitioning between monolithic parts and package**, an extended material and process **characterization** and **accurate mechanical, thermal and electrical static and dynamic models**

6) **testing of heterogeneous systems** needs definitive R&D efforts: **fault models** are missing for advanced DSM processes and for **mixed signal** circuits. In the case of embedded **RF circuits** testing is made more difficult by the long range interference in the signals, while **MEMS** testing is using empirical correlations without accurate fault description. Finally **no test model** is provided **for SiP** where basic assumptions like KGD are questionable

7) **development of advanced technologies for Systems in a Package** has to provide solutions to the **reduced mechanical stability and heat conductivity of the Cu/low k** interconnection system, to the introduction of **new materials for rf components**, to the request for higher density interconnects by the increased use of **low cost area array wafer-level packaging** and of **fine pitch and multilayer technology on flexible substrates**

8) ultimately **true 3D integration** has to be developed with special emphasis on the **thinning** of chips and wafers and their **handling**

9) owing to the growing importance of the **power sources** in the portable market, the heterogeneous systems should integrate the power devices and power management in their **design flow** (hardware/ software co-design, integration of dedicated technologies for converters and regulators) and their **fabrication** (miniaturization, CSP and WLP of power sources and power electronics). Special focus would be on **micro fuel cells**, **solar modules** and **mechanically flexible power sources**, which are **area distributed**.

10) for all these new technologies an **environmentally compatible manufacturing** has to be proven

INTRODUCTION

In the coming decade silicon devices will be divided into two main categories:

(1) bit rate performance driven digital ICs, following Moore's law on the ITRS[1] roadmap, for which the US area is dominant

and

(2) mixed signal heterogeneous devices driven by cost and also other requirements such as low energy dissipation and integration of various technologies, where Europe may have a strong leadership.

The second category of devices follows a more diversified roadmap where the minimal dimension of the transistor is only one of the key parameters of the technology along with mixed-mode or RF components, embedded MEMS and bio-functions. For this category, **heterogeneity on silicon or in a package** is the main feature for system integration.

Due to the growing importance of heterogeneous systems for the European semiconductor industry, a subcommittee of the MEDEA+ Scientific Committee has been formed, with experts from CEA-LETI, Fraunhofer Gesellschaft (FhG) and IMEC. A contribution from industrial experts was added at a later stage.

The mission of the subcommittee on heterogeneous systems is:

- to identify key issues and challenges of heterogeneity on silicon,
- to give recommendations for the priorities of future R&D programs in line with the strengths of the European industry, research centres and universities in this field.

For the sake of simplicity, this study focuses on silicon technologies, ***excluding optical devices and systems****, as well as* ***flexible electronics*** *(e.g. on plastics)*. In the same way, harsh environment(s) requiring dedicated technologies are not specifically discussed. It should also be stressed that **embedded software** is not detailed in this document, though it contributes to a large extent to the final cost of the system.

Many important applications for heterogeneous systems fit in the '**Ambient Intelligence**' (**AmI**) theme, where integrated systems are defined as smart devices which are conscious of and self-adapting to their environment while communicating with a dynamically reconfigurable network of other devices. Ultra low power dissipation for a given bandwidth and/or computational efficiency is a specific requirement for these applications and this necessitates both technological and design innovations. Technological challenges include

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[1] The meaning of acronyms can be found in the Glossary at the end of this report

extremely low-leakage CMOS, high quality RF devices (passives, MEMS, etc.) and new packaging solutions. The major design challenge deals with the co-design of programmable and reconfigurable multiprocessor architectures with distributed memories and including embedded software, broadband radios, etc..

For the longer term, completely three-dimensional packaging solutions of chips coming from extremely heterogeneous technologies must be developed as sketched by the "e-grain" or "smart dust" concepts. Here, novel power sources based on thin film batteries, fuel cells, inductive coupling or various MEMS concepts must be considered, as well as sophisticated physical and (bio)chemical interfaces to and from the outside world. The ability to exchange a broad range of complex design parameters between devices from different technologies, packages, and system in a concurrent co-design targeted towards lower cost will be an extraordinary challenge, needing to close additional technical and cultural gaps through a multidisciplinary approach.

This study uses Ambient Intelligence as a leitmotif for the underlying systems, as it helps to cover most of the expected developments of the coming years. Other important fields of applications for heterogeneous systems, e.g. image processing for augmented reality in consumer applications, bioelectronics and optical systems may require dedicated developments which are not described in the present document.

The major technology directions are covered in this document along two broad domains, namely the **system design** side, with a specific discussion on **test**, and the **system packaging technology**, with key focus on the wafer level packaging, the vertical integration and the System-in-a-Package concept, adding a specific consideration on the **integrated energy supply**. Future R&D requirements are discussed in each section.

The report is intended to be neither a roadmap nor a market study, but rather to describe various scenarios for the next decade in the field of heterogeneous systems on silicon or in a package including an analysis of the strengths and weaknesses in Europe. The conclusions of the subcommittee are summarized as a list of recommendations in an Executive Summary which is appended in front of the present document.

I. System integration of heterogeneous components

I.1. General comments

Systems isn a broad sense can be any integrated approach for achieving a given function. In this report, we consider only integrated systems which have the following characteristics:

- the system can be spatially localized (for example, a telecommunication network system doesn't fit this definition)
- applications drive integrated systems with small size and low weight, pushing the components of this system to be integrated in a small volume
- the system handles the interaction with the outside world: there is thus a need for non-digital technologies at least for interfacing the system with the analog world, even though more and more functions are implemented in the digital domain
- considering the different ways a system could interact with the outside world, it could induce a stronger diversity or **heterogeneity** in the system's subcomponents

In summary, the systems we will consider in this report bring together diverse functions and technologies, which should be integrated in a small size system (**Fig.1**).

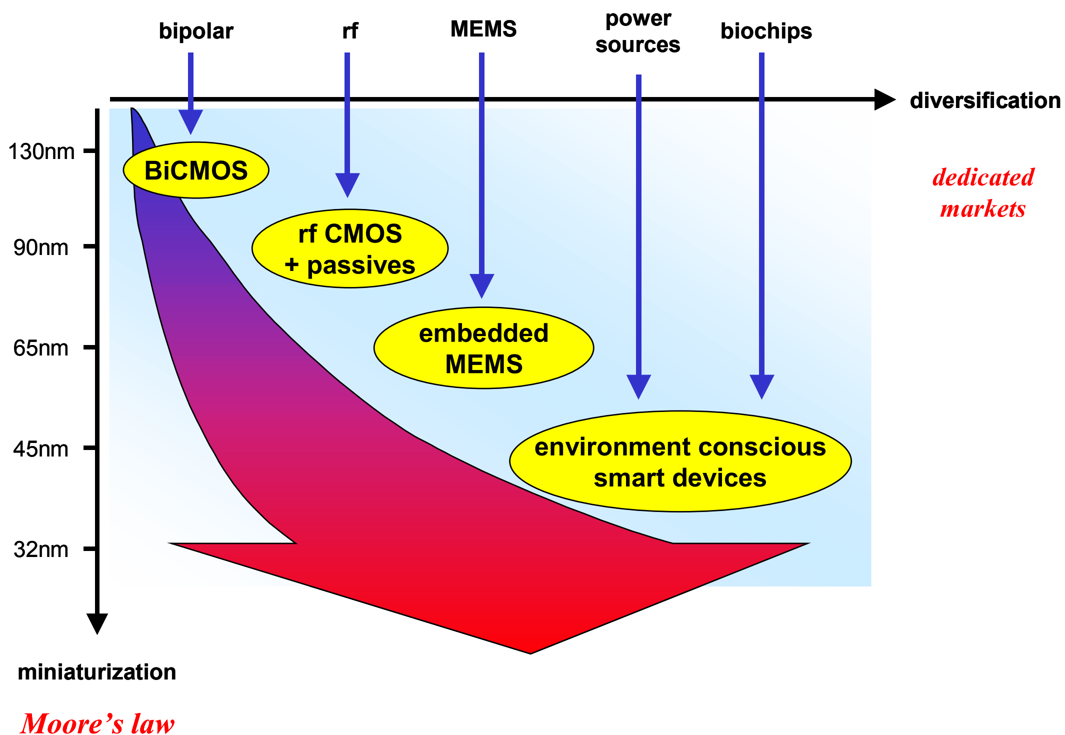

Fig.1. Heterogeneity as a general trend

The way this integration will take place depends on many different factors like the time-to-market of the product, the available expertise, the development time and cost, etc. In any case, the final product will consist of (s.**Fig.2**):

- one or many different circuits, integrating diverse functions and technologies (deep submicron processes tend to be more and more complex as they have to handle simultaneously low voltage digital computation and some interfacing with the outside world at higher voltage)
- a substrate or package which will allow the handling of the product, while protecting it from its environment

The two extreme situations are:

- a system where all the functions are integrated within a chip (the so-called "**System on a Chip**", or **SoC**): in this case, the system will be the combination of a very complex chip with a more standard package
- a system where the different functions are implemented on many chips using different technologies; all these pieces will be integrated in a complex package or on an advanced substrate in order to fulfill the system's function: this is the so-called "**System in** (or **on**) **a Package**" (**SiP** or **SoP**)

design
test
above IC & WLP
System in Package
System on Chip
in IC
manufacturing
market
advanced substrate/ package

Fig.2. Integration of heterogeneous components with advanced substrate or package in a system

From this very general introduction, it can be derived that SoC and SiP are not to be opposed, but that there is a continuum of technological solutions to bring an integrated system in the market place.

I.2. Some examples of heterogeneous systems

The multichip module (MCM) and its development into complex SiP solutions increase the system performance while at the same time reducing cost and volume. They are also paving the way for the integration of chips from different production technology backgrounds.

I.2.a Integrating different ICs in a package

The IC's, different type of memories (e.g. flash) and passive components (including rf functions) can be brought on a substrate as one functional integrated system (s.**Fig.3**).

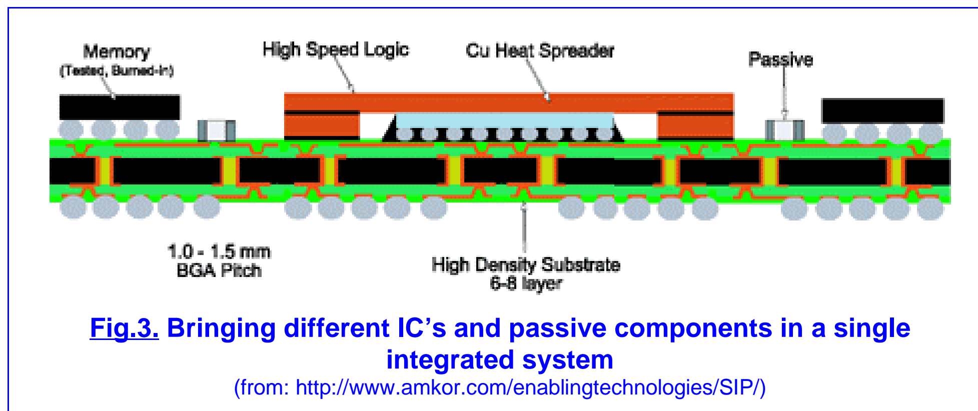

Fig.3. Bringing different IC's and passive components in a single integrated system
(from: http://www.amkor.com/enablingtechnologies/SIP/)

They may sometimes have differences in dimension to an extent which makes it possible to reduce the entire system to the area surface of its largest component, using 3D-integration techniques(s.**Fig.4**).

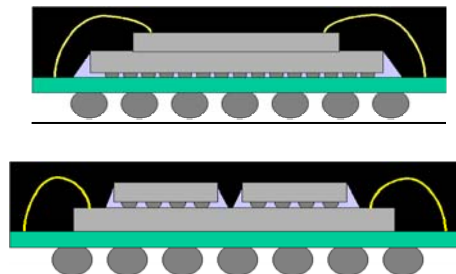

Fig.4. Stacking different components in a single integrated system (two types of stack: flip-chip and chip & wire technologies)

I.2.b Packaging MEMS with the associated electronics

Interfacing with the outside world may need the integration of the electronic data processing and software with non-electronic devices like MEMS in order to sense and act on the environment, e.g. in a mechanical way. The packages should have standardized interfaces for their mounting surface and I/O-array, and possibly also an outside geometry adapted to the application, allowing, for instance, the atmosphere to reach the integrated sensor in a pressure sensor or featuring mechanical alignment assistance to facilitate the assembly (s.**Fig.5** and **6**).

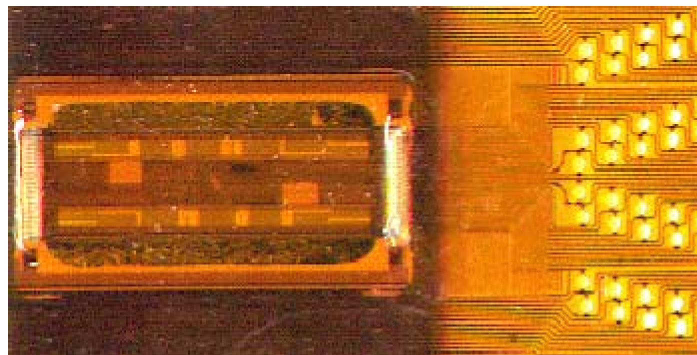

Fig.5. HP ink jet cartridge as an example of MEMS (or micro-mechatronic) package

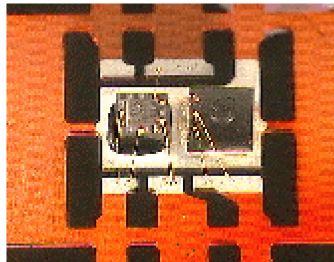

Fig.6. Microphone and ASIC chip on Cu leadframe
(from: http://www.cdnet.edu.cn/mirror/singap_college/www.ime.org.sg/adv/adv_mems.htm)

I.2.c Smart-card-packages

A special group of SiPs is not connected to the outside world via permanent electric and mechanic contacts: these are the so-called Smart Cards and Smart Labels. They are connected with read-write-devices via outside contacts (modules) or via electromagnetic fields. Their configurations cover a particularly wide range, reaching from ISO-cards and printed labels via key-chains and coins to glass tubes for the identification of animals.

For all cards without contacts, the basic components are the same: transponder-IC, microcontrollers and memory elements, and possibly antenna, some passive elements, an integrated energy source, foil displays and keyboards (s.**Fig.7**).

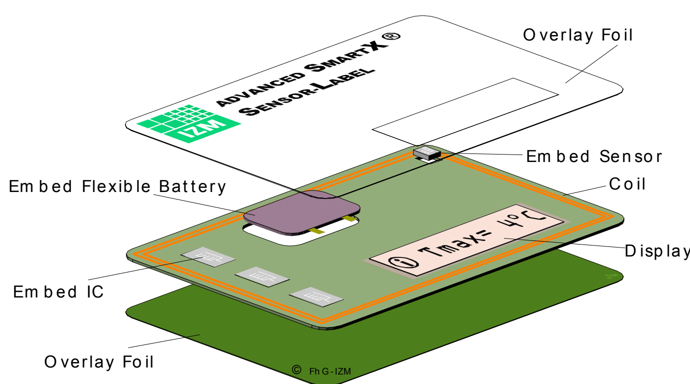

Fig.7. Multifunctional Smart Card with display and battery

I.3. Market demands for SoC and SiP

Existing markets for integrated heterogeneous systems include wireless devices, networking and computing, optical systems, MEMS systems and memory applications such as smart or flash cards. The different parameters to be taken into account in order to partition the system among the right components and technologies are:

- ***Size:*** Integrating on a single die reduces the size of the system. However, in many cases, the technology doesn't scale much (e.g. analogue parts, MEMS, etc.), reducing the size benefit while using a significant fraction of the Si area produced with a deep submicron process will increase the system cost.
- ***Technology complexity and cost:*** Integrating different technologies on a same chip can be very costly, e.g. in the case of embedded memories: it should be justified by enhanced performances for a given application
- ***Electrical performance:*** Performance is enhanced through shorter interconnections between ICs in a SiP; e.g. by placing the logic and memory chips close to one another for memory data speed enhancement. On the other hand, the higher number of internal I/O's

in the system increases the Si area consumption (e.g. through the ESD protection), the power consumption and reduces the maximum usable frequency.

- ***Thermal management:*** Often, common heat sinking approaches can be used with SiPs to minimize the number and handling of individual thermal solutions.
- ***Testability:*** While Design for Testability has made a lot of progress, allowing the testing of different parts of the die (memories, datapath, etc.), it may be more efficient to use in some cases well characterized subcomponents which are packaged together in an integrated system. On the other hand, the Known Good Die approach – when available - is progressing slowly and there is still significant cost issues (clean room, burn-in, etc.)
- ***Volume production:*** depending on the expected volume to be produced, integrated technologies can be more cost effective, SiP being for now less fitted for mass production while allowing more flexibility.
- ***Time to market:*** It is often faster to combine ICs in an SiP than it is to implement SoC at the IC level. It is also faster to make changes to the system at the SiP level than to change the entire mask set of an SoC solution. On the other hand, for high volume production and/or performance optimization, an SoC approach can be more effective.

SYSTEM AND DESIGN ISSUES

Hugo De Man, Jo Borel and **Robert Mertens**

Introduction

In the coming decade silicon devices will be divided into two main categories:

- very high clock rate microprocessor structures for high end computing and servers following the traditional aggressive scaling on the ITRS roadmap for raw speed;
- mixed signal heterogeneous device architectures for wearable consumer electronics and pervasive computing and communication. These devices are driven by other requirements than raw compute speed such as low energy dissipation, integration of various technologies and, above all, low cost.

The second category of devices follows another roadmap in terms of transistor parameters (e.g. low leakage prevails over high speed). Here, diversification within a given technology generation, defined by the minimal half pitch, is important and includes e.g. BiCMOS, SiGe transistors, rf-CMOS with integrated passives, multi-V_t devices, novel memory technologies such as MRAM or FRAM, embedded MEMS and chips with bio-functions. Typical fields of applications for such heterogeneous systems are in virtually all non-PC devices that combine computing, communication and consumer electronics into the creation of Ambient Intelligence [2] [3]. A very important sub domain of this will be the application of electronic microsystems to the future problems of health and comfort in future society where biological systems will be connected to electronic control and intelligence.

Where the first category is the traditional driver of US dominance in the computer field, the second category fits a traditional domain of strength of the European system-oriented industry. Hence the ability to design cost-effective heterogeneous micro-systems is crucial for Europe's electronics industry.

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[2] D. D. Buss: "Technology in the Internet Age", Digest of technical papers ISSCC 2002, pp. 18-21

[3] F. Boekhorst: "Ambient Intelligence, the Next Paradigm for Consumer Electronics: How will it affect Silicon?", Digest of technical papers ISSCC 2002, pp. 28-31

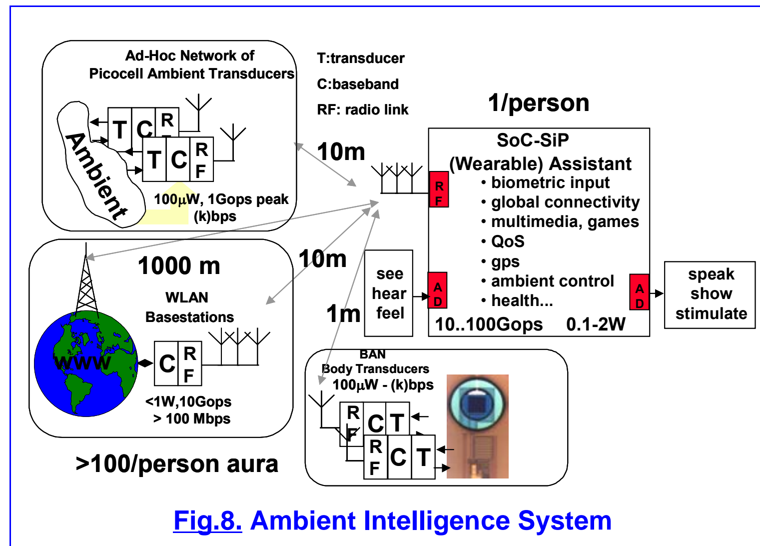


Fig.8. Ambient Intelligence System

Fig.8 sketches what an Ambient Intelligence system of the future could look like. Every person will have a personal SoC or SiP wearable assistant with biometric input, *seamless auto-adaptive* wireless and *broadband* connectivity to the web, to the ambient and to the own Body Area Network for health monitoring, security and biometric interaction.

Natural interfacing to speech, pictures, gestures and graphics requires *full multimedia capabilities* that auto-adapt the QoS to the communication channel, computing resources and main attention span of the user. GPS is needed for navigation.

There is a wireless connection to the ambient, which consists of a picocell ad-hoc radio network of transducer nodes. The latter are *low bit rate* ultra low power (<100µW) radio transducer systems that get their energy from the environment. The same technology can be applied to the Wireless Body Area Network (WBAN) where use is made of bio-transducers. Notice that the wearable assistant has to perform a set of concurrent, real time tasks that have to *adapt* to both the user's wishes and the services provided by the environment. Therefore such a system must be *flexible* (programmable and reconfigurable). In contrast, WLAN and certainly WBAN and ambient nodes are more ASIC like devices with a *fixed or parameterisable* functionality, ultra-low cost and energy consumption.

In order to derive strategic domains of research to design optimal heterogeneous systems for this domain we first derive the challenging system requirements for these micro-systems in **section II**.

In **section III** we will derive the challenges to design methodologies and design organization, with critical missing technologies.

Finally, in **section IV** we identify a number of priority R&D topics as well as a suggestion on how to organize system level design research in this domain.

II. Ambient Intelligence System requirements and challenges

II.1. Ambient Intelligence leads to heterogeneity

Each component of the Ambient Intelligence system is *embedded* in a global system environment (network, sensors, actuators, users, appliances). An Ambient Intelligence component may be a micro-system in itself containing rf, analog signal processing as well as digital signal processing and communication protocols. For reasons explained below, the latter are to be implemented on novel programmable or reconfigurable *platforms* predominantly under the form of *embedded software* that is either part of the specification or it is consists of *downloadable embedded software,* that adapts the system to a new environment, mode of operation, new standard or new application.

So these systems are characterized by:

- heterogeneous specifications
- heterogeneity at the chip level (SoC=rf + analog + digital + software + power supply)
- AND/OR heterogeneity at the package level (SiP)

Key to this is diversified CMOS, MEMS, biosensor and packaging technologies and appropriate design methodologies to cope with the mapping of heterogeneous system specifications into the novel degrees of freedom in implementing them in that novel manufacturing technology while satisfying the stringent low power and cost constraints on ever increasing computational complexity of these systems as discussed below.

II.2. Power efficiency requirements

Today's microprocessors (µP) execute about 3 Gops for 30 W of power or a *power efficiency* of 0.1 Mops/mW. This is unacceptable for e.g. a wearable Ambient Intelligence assistant that may require a peak performance between 10 to 100Gops for 0.2 to 2 W to get an acceptable battery life of about 50 Mops/mW.

This is 500 times the power efficiency of a µP.

The situation also applies to WLAN base stations that will provide multi-user shared bandwidth in excess of 100Mb/s. Such systems are to be mounted in every room and should not burn more than 1 W for 10 Gops or 10Mops/mW to reduce packaging cost.

The biggest challenge comes from the transducer nodes that live on ambient energy (vibrations, body heat, light etc.) yet perform sophisticated ad-hoc radio protocols. Their digital power efficiency is estimated at 100Mops/mW such that, with the RF part included, average power stays below 100 µW.

In conclusion:

- Clearly, for the digital part, we need power efficiency that is 100 to 1000 times higher than for today's PC microprocessors. This will not come from simple technology scaling alone but it will require *disruptive new architectures* whereby flexibility is a key requirement certainly for the user terminal.

- This is not sufficient though since also for the rf parts we must come up with novel ultra-low power radio *system* architectures and obviously this requires again *a global system design approach from link budget all the way to a best of breed heterogeneous technology implementation*. (Most likely the best solution will not be an all CMOS radio!).

II.3. Growth of computational complexity

One can wonder why computational complexity will go up for non-PC, non-Server applications. The reason is in the advances in spectrally efficient and broadband communication as well as non-keyboard human. The widespread use of broadband wireless connectivity requires indeed the ultimate of spectral efficiency (bps/Hz) i.e. we must approach Shannon's limit. This leads to a huge increase in algorithmic complexity for channel coding, channel estimation, detection of multi-user signals and for multi-array antenna systems. E.g., in going from 1G to 3G wireless, computational complexity increased from 10 Mops to 13Gops

On the other hand, we need to use the most advanced compression technology such as MPEG4-21 that allows for scalable compression with adaptive QoS but requires up to 5Gops for high quality video.

The strongest requirements come from human interfacing. Speech recognition, language translation and biometrics require real-time database searches with up to 100 G data transfers/sec while 3D graphics, games and video indexing can require up to 100Gops. How this will have to be distributed over the network is part of the global system design issue.

Conclusion:

The computational complexity, even from a wearable Ambient Intelligence terminal, will be an order of magnitude above today's GHz clocked microprocessor *but it must run at 1/100 of the power density of it. In section III we show that this requires novel multiprocessor chip architectures with clocking, power and* V_t *controlled by the real time operating system for these architectures.*

II.4. Real-time memory-intensive systems

Non-PC systems are dominated by real-time stream based processing of multi-dimensional data or packets.

Hence they will be memory intensive. Up to 80% of these devices will consist of a hierarchical memory architecture most of which will have to be embedded to save power in the data transfers. Technologically there is a great need for novel cheap, voltage scalable, low leakage embedded memory and design technologies for optimal memory hierarchies. *On the other hand novel 3D packaging SiP techniques may offer a new degree of freedom in creating cheaper systems by not diversifying logic CMOS process with specific add-ons but by e.g. using a 3D connection to specialized low leakage Video DRAM's off the logic chip. This may lead to higher yields, lower cost, and better performance but will introduce new challenges to the test problem.*

II.5. Software IP and the design gaps

Although process and packaging technology deliver a necessary component to building Ambient Intelligence systems, it is by no means sufficient…*the devil (and the cost) will be in the software.*

In practice, all of the above system algorithms (components of the specification) are developed by *system engineers* or *standardization groups.* They are available as *software IP* written in standard programming languages such as C, C++, MATLAB or SDL to show well-documented executable *functionality*. Generally, no attention is paid to their implementation efficiency in low-power hardware/software architectures. System engineers are not used to apply clean models of computation that would help efficient compilation into target architectures. At an even higher level, *service engineers* will embed these software IP's into *user scenarios* for services offered on Ambient Intelligence systems. As shown in Fig. 2 these *software centric system specs* have to be mapped into energy efficient, yet flexible architectures in deep-submicron and/or nano-technology.

Who will do this? Who will have these skills or who can be trained to acquire these skills and who can train in a discipline that does not yet exist?

Indeed, today's *chip designers* have just now mastered HDL based RT-level design and, at best, IP based design of bus based hardware/software platforms based on emerging C-based specifications.

However traditional chip designers are usually not too familiar with the application domain at the system level while DSM scaling itself creates a whole set of novel physical phenomena as shown in **Fig.9** that have a deep impact on IP and chip architectures.

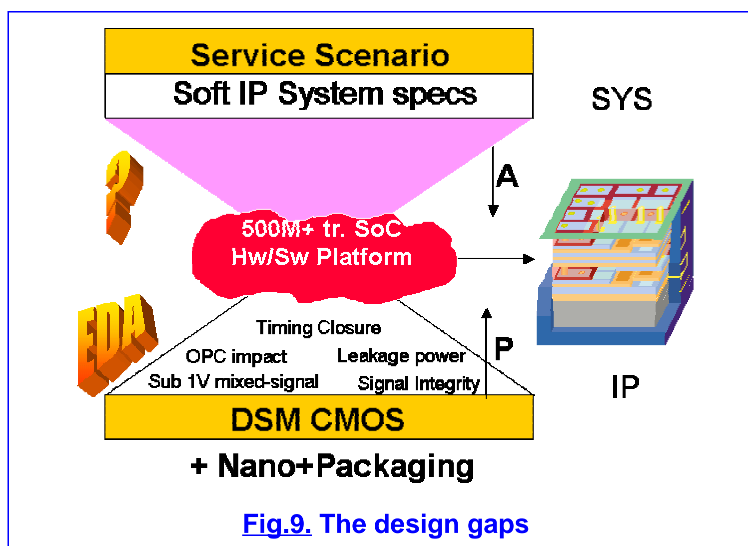


Fig.9. The design gaps

From the 130nm node on (today!), library and tool designers have to rethink hard IP libraries, analogue design styles and *back-end design tools* to cope with these phenomena. This is the so-called *physical gap P* in **Fig.9**.

This is a rather generic issue for the technology, IP and CAE vendors and CAE vendors are already heavily investing in these back end tools, as their generic nature must guarantee a return on investment in tool and library development. We believe that this gap will be filled soon by the US tool vendors.

However, the biggest bottleneck will be the *architectural gap* A in **Fig.9**. This is a gap whereby a *new breed of designers and tool developers* is needed. They are *domain specific SoC-SiP architects* able to cooperate with the system and service engineers to *refine* the software IP specifications into low cost, low energy hardware/software SoC's or SiP's embedded in the global distributed computing network.

Conclusion:

- Most likely, process technology will not be the showstopper to Moore's law but the availability of adequate design methodologies and enough SoC-SiP architects skilled to apply them to the design of Ambient Intelligence architectures that will make the difference.
- The difficulty here will be to formulate *concurrent research and education projects in system design methodology and technology for heterogeneous systems.*
- This requires a new collaborative and multi-disciplinary approach to system level design and technology research driven by well-chosen long term application domains as described in[4] and applied now in a number of initiatives worldwide[5]. There will be no success if research is too scattered and not driven by a well-defined common goal with a sufficient long-term component.

III. Heterogeneous system design challenges

When one looks at the relative market position of the ASIC (fables) companies and IC companies (IDM) few years after design implementation, a key factor was their capability to implement complete design methodologies, including the quality of the design flow (relying mostly on cooperation with EDA vendors), the capability to handle diverse technologies and advanced deep submicron processes, IP's, engineer training, etc. It is thus of utmost importance for European companies to participate in and support advanced R&D in the design of heterogeneous system through R&D centres and start-ups.

III.1. A paradigm shift in design requirements and cost

In contrast to PC processors, raw performance will not be the driver of heterogeneous systems for e.g. Ambient Intelligence, but *lowest energy consumption for a given performance and flexibility requirement*.

[4] H. De Man, "System-on-a-Chip Design: Impact on Education and Research ", *IEEE Design & Test,* Vol. 16, No.3, pp.11-19, July-Sept. 1999.

[5] See e.g. Berkeley Wireless Research Center: http://bwrc.eecs.berkeley.edu/ or Yamacraw Initiative: http://www.yamacraw.org/ or Gigascale Silicon Reseach Center: http://www.gigascale.org/

This asks for a *global design approach for system optimization* as most power reduction in wireless systems depends on the overall communication set-up and as we are looking essentially at globally distributed applications. Furthermore, achieving low power at the component level, requires attention at all levels of design from specification to layout and packaging.

In addition, the hardware cost of Ambient Intelligence systems should be less than 1€ for transducer nodes and 50€ for personal assistant nodes. We may even approach the point where *silicon is free and the money is made on services* offered on the silicon platform. Hence, much more than for infrastructure and traditional computing, cost reduction is essential. Since for DSM SoC systems actual NRE costs are exceeding 10M€ it is clear that design methodology research to reduce NRE cost is crucial for the exploitation of future process technology.

All systems will be *mixed-signal* systems, possibly containing rf and base band, if not on the same chip, at least in the same multi-chip package. Again, this partitioning requires a *multidisciplinary team based approach* between service, system, SoC architects, IP providers and CAE specialists.

Conclusion:

At a time of an increasing desegregation of the industry, there is a definite need for a holistic approach to the design of systems that have a high degree of heterogeneity. Success in this area will depend on our ability to organize collaborative research and ways to organize collaborative design over all levels of abstraction. Just like the huge cost of future process technology requires a sharing of development cost, we may need a similar activity in the design arena.

In the sequel we discuss design challenges for heterogeneous systems at the chip level and the packaging level.

III.2. Design challenges for heterogeneous systems on a chip

III.2.a The digital design challenge: the need for disruptive digital architectures

Getting 1 to 2 orders of magnitude gain in power efficiency for data-transfer dominated Ambient Intelligence systems requires in the first place a *rethinking of domain specific computation architectures.* The ability for fast hardware *and* software design of these novel architectures will be the key product differentiator between competitors. Basically, we can make a distinction between the *cheap, ultra low-power transducer nodes* and *more expensive, low-power personal assistant devices.*

The first implement small base band communication systems in the order of *10M transistors* with *little flexibility* (parameterisable blocks or simply duplication of hardware on a pad-limited chip). Active power efficiency in excess of 100MopsS/mW is required.

The latter are very complex systems (>100 MTr) with a high degree of *domain specific flexibility.* Flexibility is defined as *programmability and (dynamic) reconfigurability.* Yet power efficiency better than 50 MOPS/mW is required.

Both systems should have negligible static leakage power in standby.

For data dominated systems, most of the power dissipation results from data-transfers to and from memory. New architectures with orders of magnitude better exploitation of memory hierarchy and of spatial localization are necessary. New platforms consisting of networked adaptive computing machines will be needed.

Research in this area should focus on:

- design methodologies for ultra-low power multiprocessor architectures (typ. 100 processors @ 200 MHz) for domain specific programmable, memory dominated platform. This includes spatial / temporal localization of the data production and consumption with special attention to design methods for low power memory hierarchies and localizations. This also involves on-chip and inter-chip networking making use of interconnects hierarchy.
- efficient ways to optimize the partitioning between hardwired, reconfigurable and programmable parts in term of performance, power, cost and time-to-market (service/ architecture/ compiler co-design)
- efficient ways to generate low power programming and compilation and middleware environments for such systems.
- efficient ways to generate automatically RTOS systems for dynamic task assignment and power control e.g. by frequency and/or V_{dd} control.
- novel DSM compatible logic and wiring fabrics (reducing e.g. OPC cost).
- introducing leakage reduction techniques at chip and IP level (leakage of DSM processes may dominate active power).
- …

III.2.b Some specific areas of development in design methodologies

Beside deep submicron technologies needed for reducing power consumption of devices with increased functionalities, mixed signal and rf parts will be found everywhere in these systems dominated by connectivity and interfaces with the outside world.

i. Deep Submicron CMOS

In deep submicron technologies, the supply voltage is strongly reduced, leading to a lower active power consumption (as required), but also to a lower noise margin. If logic blocks are added to compensate this drawback (e.g. with error-correcting codes), the final active power consumption could be higher than with previous technologies.

On the other hand these technologies allow more connectivity and new slogans are emerging like ‘work on interconnect-centric design’ or ‘don’t route wires, but data’!

Once again, deep submicron CMOS leads to a renewed approach of design and not in a ‘business as usual’ method.

ii. Mixed signal

All Ambient Intelligence systems will have radio and mixed-signal parts that take as much design time as the digital part of these systems. A difficult challenge for the monolithic SoC approach is that digital CMOS, analog CMOS, passive components and the various sensors

and actuators follow different scaling laws. Therefore important design trade-off's must be made. Moreover, substrate noise caused by the unavoidable inductances in the power and ground tracks is a major problem, especially if the supply voltage is scaled down to achieve ultra-low power dissipation.

There is a definite need for development of:

- Novel overall mixed signal architectures where the need for analog precision is compensated by more digital techniques and dynamic power management.
- Novel mixed modeling and simulation techniques that allow e.g. the simulation and analysis of complete rf architectures from link to baseband processing.
- Development of design methodologies and analysis techniques to reduce substrate coupling and to secure signal integrity.
- Development of test technology for heterogeneous SoC's.

iii. Ultra-low power radio's

The ad-hoc network of pico-cell ambient transducers (**Fig.8**) and the BAN (**Fig.8**) are self-contained in terms of energy via a one-time battery or fuel cell or a 'refillable supply' of energy scavenged from the environment. Therefore the average power dissipation is not allowed to exceed 100 µW. To achieve this goal, every function in the radio must be designed for maximal power efficiency. A multi-hop ad-hoc network approach is probably necessary, avoiding the use of high-power gain amplifiers. For integrability, higher frequencies allow smaller passives and antenna and therefore ultra-wide band transceivers are attractive. Development of ultra-low power passive filter MEMS can be a solution to reduce power in such architectures.

Development is needed on:

- accurate macro-modeling of the channel, the front-end and the base-band parts
- efficient verification and simulation environment
- digital compensation of non-idealities, esp. in the channel and front-end parts
- efficient model and simulation of the signal integrity (e.g. substrate noise)
- efficient portioning between monolithic parts and package (e.g. high-Q passives)
- …

III.3.Specific design issues for Systems in a Package

Novel packaging techniques are emerging at a fast rate. These techniques, if cost-effective, can be an excellent engineering approach to avoid the costly process extensions of digital CMOS to include rf devices (BiCMOS, SiGe), high Q inductors, high voltage transistors, DRAM cells, etc… This leads not only to ever more expensive (and lower yield) CMOS processing but also to extremely difficult design methods to circumvent trade-offs at all levels of system design. This adds considerably to NRE cost and excessive time-to-market. Therefore research is needed to develop design methodology to exploit these novel degrees of freedom in designing heterogeneous systems.

First of all, existing methodologies for SoC design must be adapted to the additional degrees of freedom introduced by the SiP approach. How can the IP based SoC design methodology

be generalized to SiP? Additional R&D challenges are the development of a sufficiently generic and affordable testing methodology and methods for built-in self test. Reliability issues must also be taken into account during the design phase.

Conclusion:

Though part of the present topic is covered by the MEDEA+ Design Automation Roadmap, the challenges for heterogeneous system design calls for a 'total' design approach, including the whole supply chain from the system and device design to the fabrication and packaging and to the multi-scale modeling of the different technologies (s. **Fig.10**).

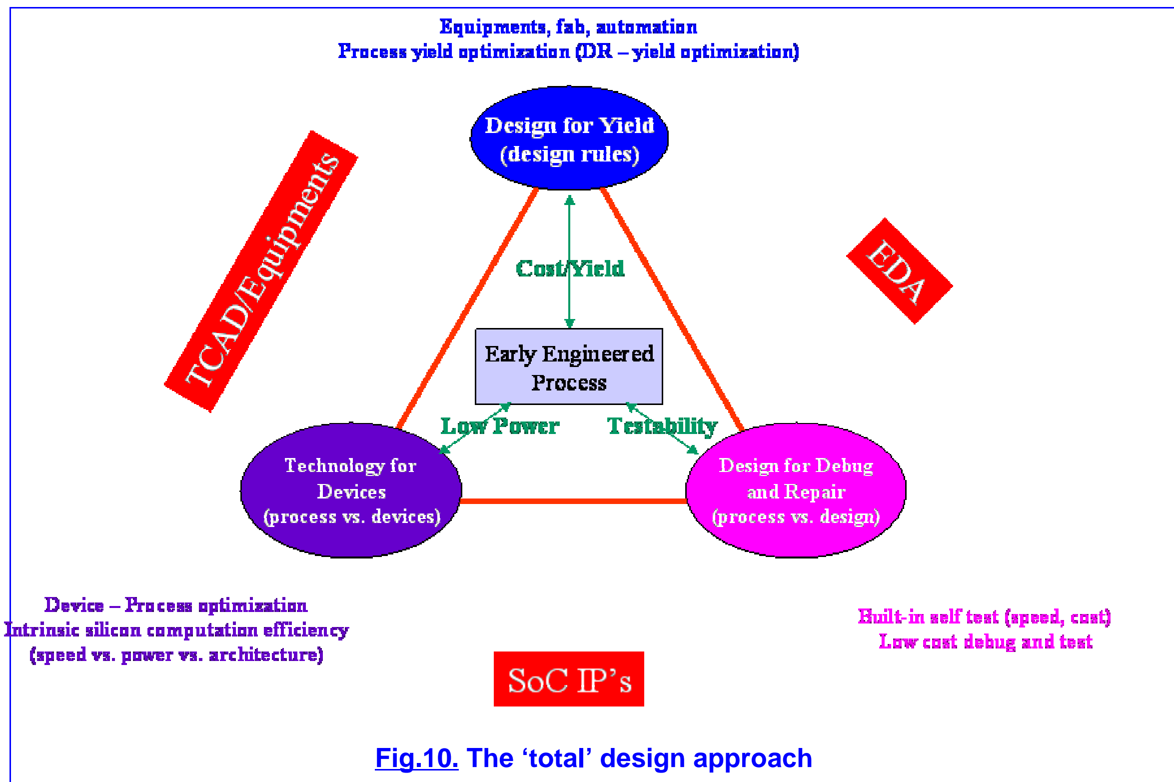


Fig.10. The 'total' design approach

IV. The need for collaborative research at the system level

At the 30 nm level nano- and microelectronics will meet around 2010. Even if further scaling would be problematic, the system opportunities for future societal information systems become virtually limitless and the challenges to design around the electrical effects of nano-scale devices become formidable. On the other hand, the merger of different techno-cultures offers ample opportunities to make Marc Weiser's dream on Pervasive Computing and Communication or Ambient Intelligence come true.

However, it will not be business as usual by just doubling transistor count or clock speed. Most likely, progress will be the result of merging presently unconnected domains and techno-cultures to create the ultra-low power, low cost, always connected devices operating on novel energy sources for as long as the system's lifetime. In contrast to the past, and contrary to the usual techniques of managing complexity, worlds ranging from advanced

software like AI down to molecular electronics will have to merge to build these systems. *So, more than ever before, we must create mechanisms for dialogue to bring design oriented people together, join in acts of creativity and thinking on how to organize a dialogue to facilitate design methodology over the discipline boundaries. A great result could be that they at least understand each other's terminology and way of thinking.*

Some examples:

- Plastic Electronics: Throwaway electronics in medicine, smart pills, smart security tags, smart walls, flexible displays, plastic solar cells, chemo-sensors…
- Merging bio-molecules to silicon sensors and intelligence. Design in four layers (bio-molecular-sensing-intelligence)
- Designing novel e-grain architectures in ultra-thin silicon in 3D silicon structures and interconnect architectures (layers of antenna, sensors, RF, base-band memory, intelligence and energy provision)
- Ultra-low power intelligent memory architectures for AI searching systems
- Artificial senses….

This requires a "vertical" organization of system level research organized around well chosen strategic application domains with a sufficient long-term perspective. The best formula is probably the creation of Focus Centres of Excellence of sufficient critical mass to support multidimensional teams to create demonstrator designs showing the feasibility and cost issues of design methodologies in a given process technology. At the same time such centres should be networked with the scientific community and results should be available for dissemination to the system design community (s. **Fig.11**). Progress will no longer be possible by peephole optimizations within specialized domains.

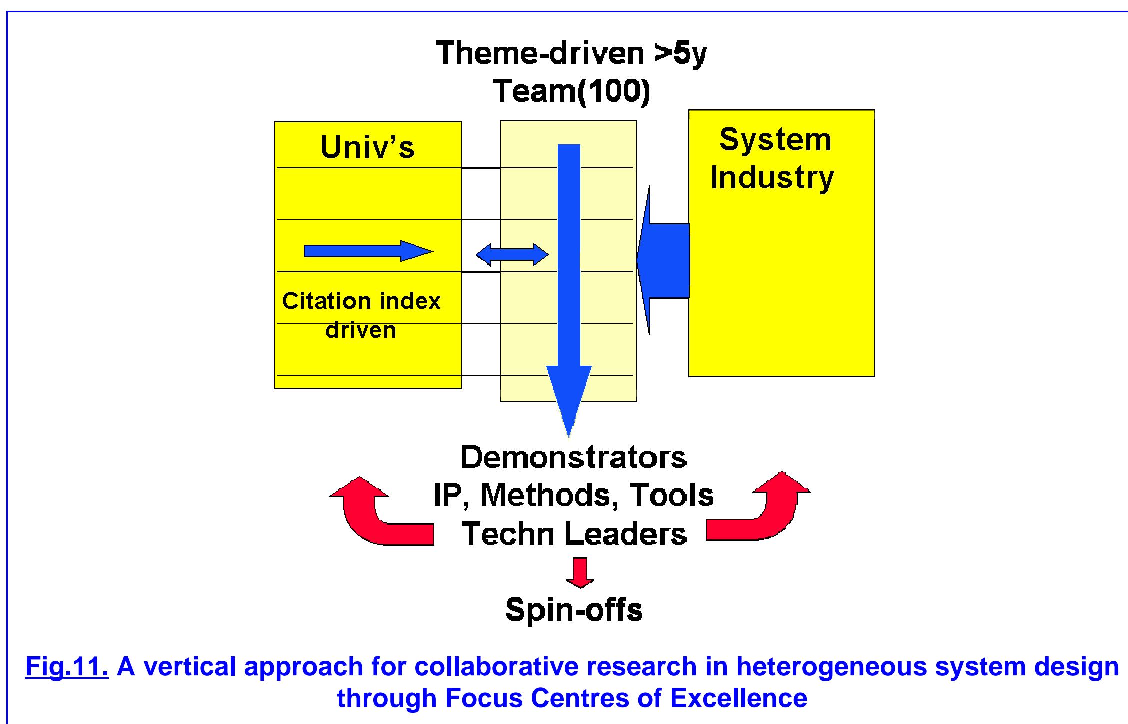


Fig.11. A vertical approach for collaborative research in heterogeneous system design through Focus Centres of Excellence

TEST

René Segers

We consider here manufacturing testing, not design verification, nor software testing, both which can be done (at least partly) without actual silicon. The strategy of this kind of test is to use a known fault model in order to provide a given fault coverage and EDA support.

Testing serves various purposes:

- to distinguish between good and bad dies/ SiPs, but also to asses those parts that pass the test but are suspect to fail shortly (reliability issue e.g. I_{ddq} in IC)
- to provide feedback on the failure modes and defects in order to improve the test procedure itself, the design and the process (yield improvement); it should be stressed that this kind of feedback is extremely useful to improve yield and cost of a given product and that it is an issue for fabless companies

The challenge is to define and to implement a common DfT (Design for Testability) and test flow(s) (s. **Fig.12**) that suits the needs of the system designers, the wafer fabs (incl. assembly for feedback in the development and production phases) and the test operation, without changing the existing equipments and tools presently used.

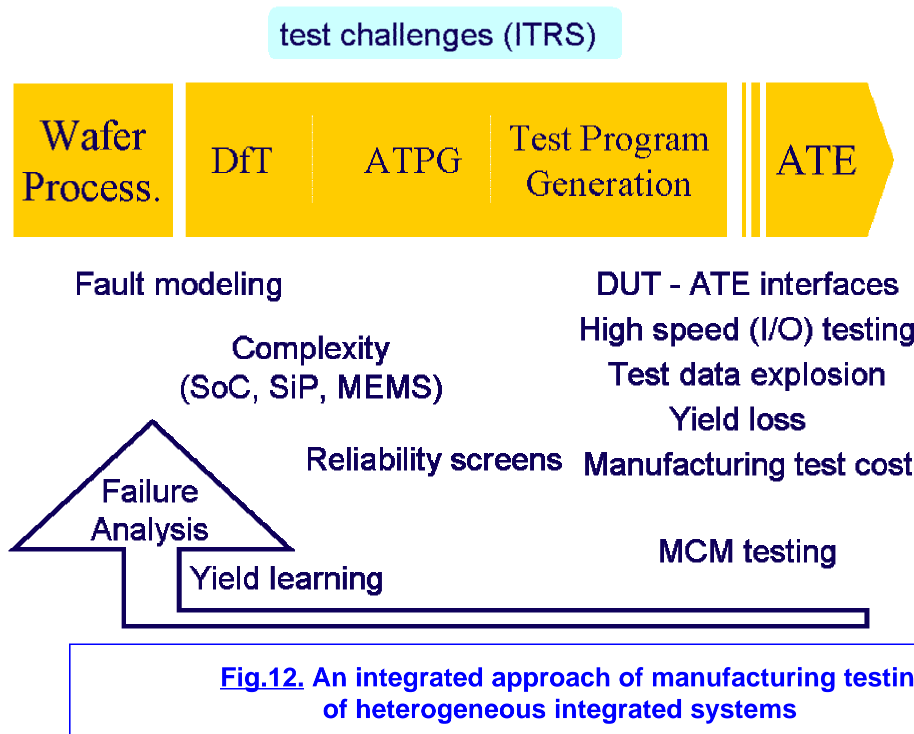


Fig.12. An integrated approach of manufacturing testing of heterogeneous integrated systems

However, as we introduce new heterogeneous systems, we encounter several problems:

- the amount of test data explodes along with heterogeneity in the way they are acquired (e.g. e-DRAM retention time vs. logic timing issue)

- circuits which can't be tested in real conditions (e.g. at speed)
- the deep submicron processes brings unknown defects which are not fully described
- in analog and mixed signal circuits, hardly any structural fault model exists:
    - o extensive functional (specification) testing is needed
    - o trial and error or legacy approach (take test from older devices) is used
    - o long test times are needed
    - o relatively expensive test equipment is used
    - o BIST approaches hardly succeeded until now (unlike in the digital domain), probably for several reasons: these approaches are too general and not specific to the mixed signal design, the pressure of the market on mixed products is not high enough for significant R&D in that field and the technical limits are not yet reached
- embedded memories require specific (self-) test approaches (one per memory type, with a lot of BIST and with bit mapping), though in principle it is "just" a core in a core based design. The main issue is to get access to detailed information in the memory array.
- embedded rf circuitry may be handled just as another core, but true test needs special access. Long range interference make testing difficult. Solution could be - as for high speed I/Os – to use some kind of feedback loop.
- the fault description of sensors and actuators is mostly missing: calibration of MEMS is a matter of empirical correlation with other electrical tests and significant R&D in that field is missing
- there is no test model for MCPs, MCMs
    - o this field is at the level of academic research
    - o the basic strategy is similar to JTAG/BIST: the dies in the package are assumed to be Known Good Dies (KGD) and one tests the total system with a Boundary Scan (like) approach
    - o however, KGD are difficult to wafer test (WT), as they are usually bought from outside and JTAG can be not implemented
    - o the consequence is that there is a mix of ad-hoc and standard test approaches, only partly supported by tools

SYSTEM PACKAGING

Jürgen Wolf, **Rolf Aschenbrenner** and **Michel Brillouët**

V. Introduction

System integration, of which packaging technology is a key element, represents an integral prerequisite for the manufacturing of future products. The idea behind system integration is to combine individual components and subsystems into a functional electronic system. The processes used need to offer solutions for the most varied areas of application. Hence the choice of technology and material as well as the system design determine size, weight, performance, user-friendliness, reliability and, finally, the price of a product and thus its market success. The increased utilization of micro-technological or even microsystem components represents a challenge for future packaging technology due to the increased functionality of products. Packaging and interconnection technology plays a key role in this context. Today's manufacturers often use standard technologies from microelectronics. Here they can rely on an established infrastructure of material, equipment and service suppliers, R&D institutions and system users. Faced with the rapid development of individual components and microtechnology subsystems, the established standard technologies will not suffice the growing demands much longer. This development is further enhanced by the need to integrate non-electrical information, such as optical, mechanical, fluidic or (bio)chemical signals.

Simulation and design technology for microsystems needs to be improved and integrated in existing software in order to achieve fast product development. Technologies available today offer a solid basis for the new product generation.

Aspects that need to be paid particular attention include:

- area array packaging (flip chip, CSP, system-CSP)
- System-in-Packages (SiP) using 3D integration technologies
- cost efficient and flexible substrate materials
- thin semi-conductor chips
- cost-efficient bumping processes
- fine pitch and multilayer technology
- integration of passive and active components into the substrate
- integration of optical and electrical signal transmission
- material characterization (model and measurement)
- as well as an environmentally compatible choice of materials and processes.

The manufacturing processes needed for the realization of highly complex and mobile future products require the integration of design, technology and quality. Terms like '**Known Good**

Die' (**KGD**), '**Wafer Level Test and Burn-In**' and '**Wafer Level Packaging**' (**WLP**) lead the way to a cost-efficient complex system packaging.

The **MultiChip Module** (**MCM**) and its development into complex **SiP** (System in a Package) solutions of maximum functionality have introduced a new level of assembly and bonding technology, simplifying the realization of optimized subsystems. They increase the system performance while simultaneously reducing cost and volume. They are also paving the way for the integration of chips from different production technology backgrounds.

VI. Wafer Level Packaging

VI.1. Definition and advantages

The **Wafer Level Packaging** process (**WLP**) is a technology in which all of the IC packaging is performed at the wafer level. A WLP technology can, for the first time, maintain the cost of the IC packaging as a constant percentage of the total wafer cost. This is possible because the cost of packaging operations is no longer assigned to the individual chip but to the wafer. A WLP technology requires that when the chip size shrinks in later years, all of the package interconnects will continuously be located within the chip outline (it must be a fan-in design, known as the real chip size package). From a systems perspective, the limitation of WLP is how many I/O can be placed under the chip and still have a board design that can be routed.

Driving forces for wafer level packaging are portable products with increased functionality and speed like consumer, e.g. digital, video cameras, communication devices, e.g. cell phone handsets or computing devices, e.g. notebook computers and PDAs

The primary application market for WLP technology is projected to be low to moderate I/O density applications, as typified by high yield DRAM, Flash, Analog, EEPROM, RF and other ICs with ≤ 100 total I/O and adequate silicon area.

CSP packages from WLP technology reached the level of practical use in 2000. Its use will expand in the field of portable devices and other small-size devices that require high-density mounting. A key enabling technology to take full advantage of a WLP will be the development of wafer level test and burn-in. Most WLPs with I/O pitch equal to or greater than 0.5 mm and with solder balls (> 300 µm) do not require the use of underfill and can therefore be directly implemented into a standard surface mount technology (SMT) process flow.

VI.2. Types of WLP

A wide assortment of technologies has been divided into four classifications categorized by the process technology used to achieve first level interconnection on the wafer as summarized in **Table 1**.

Redistribution and bump is the predominant WLP technology in use today. There are several reasons for this technology having taken the early lead. First, the thin film process technologies used in this approach are largely based on those used in wafer fabrication. They incorporate standard photolithography and thin film metal deposition/patterning techniques to

define the signal routing layer and the under bump metallurgy (UBM) for the solder ball attachment pad. Due to the relative process simplicity of redistribution and bump approaches, it is expected that they will set the price point and performance target for all new or emerging WLP technologies.

WL-CSP Bump Technology	Companies
Redistribution Layer (RDL) and Bump	Amkor (Ultra CSP™), Apack, Aptos, ASE (Ultra CSP™), ASAT Chipbond, Dallas Semi (2 lead), FCT (Ultra CSP™), Fraunhofer Institute, FuPo, Hitachi, Hyundai, National Semi (µSMD™), PacTech, Sandia Labs, Seiko Epson, SPIL (Ultra CSP™), Unitive (ExtremeCSP™)
Encapsulated Cu Post	Casio, Fujitsu (SuperCSP™), IEP, Oki Electric, TI, Shinko (SuperCSP™ license), Toshiba
Encapsulated Wire Bond	Form Factor (Wow™, MOST™), Shinko, Hyundai, Infineon (Wow‰ licensees),
Encapsulated Beam Lead	ChipScale (Intarsia, M-Pulse Microwave), ShellCase (ShellBGA™), Tessera (WAVE™)

Table 1. WL-CSP Technology Alternatives; Sources: Prismark and TechSearch

VI.3. Chip-Scale Packages – Redistribution Technique

Chip scale packages (CSP) provide a promising solution where low weight and small size are requirements. These packages are only slightly larger than the chip itself, and are available in a variety of configurations and material combinations. They provide potential advantages of higher performance, higher density, and chip shrink transparency. For applications where CSPs are redesigned to the minimum size possible, each time the chip size is reduced a corresponding redesign of the PWB onto which the packages are assembled will be required.

The packaging challenges in the RF and mixed-signal realm will become increasingly important as low-cost mobile and high bandwidth products expand across all market segments. The increasing performance of silicon SiGe, and GaAs devices coupled with dramatic device cost reductions have established the need for very low-cost, high-performance packaging. In the RF product area frequency will shift up to the 5 GHz range that will require improved dielectric loss, tighter control of parasitic variability due to process variations and more precise electrical simulation capability. Flip chip attachment to package and embedded passives on the package will be key enabling technologies for system packaging. Contrary to the traditional packages low inductance and high-density packages like FBGA/CSP will enable designers to use lower cost partitioning solutions.

VI.4. Flip Chip vs. WL-CSP

Wafer bumping is a key element of the successful implementation of flip chip technology. Eutectic Sn/Pb bumps on organic substrates represent the target against which potential solutions should be benchmarked. There are several challenges to implementation and

proliferation including cost, density, manufacturability, availability and compatibility with on-chip Cu/low κ materials. Potential solutions to reduce soft error upset from alpha particle emissions could include moving to low alpha Pb and Pb-free solders during the timeframe of the next decade. Cost for bumping a wafer (on a per-chip basis, including the under bump metallurgy and the bump deposition) needs to decrease continuously over this period through process simplification.

Any lower cost process must preserve reliability, quality, and yield. Bump pitch will decrease from 160 µm or greater today, to 70 µm by the end of the decade for high I/O and high-power chips. This will increase the wireability requirements for the substrate significantly. For low I/O chips in low-cost and hand-held applications, the bump pitch must be reduced continuously to address shrinking die sizes without degrading high frequency performance. Bumped wafers and chips must become generally available at a cost below packaged devices but at an equal quality level.

New interconnection technologies, like bumpless interconnects, will be required especially for thinned silicon devices and flexible substrates, for chip to chip and chip to wafer approaches. Special attention needs to be paid to thin barrier and active solder layers.

Testing represents the greatest technical challenge to achieve the quality goal. The test adaptor reliability must be achieved at elevated temperatures without inducing bump damage. The flip chip must be, and be perceived as equivalent to a packaged device. Achieving this perceived equivalence is the greatest short-term challenge and needs greater industry focus for success.

VI.5. Integration of passive RF components above an IC chip

An increasing part of the subsystems, e.g. in a mobile phone or in the future transducer nodes for an AmI scheme, is devoted to passive RF devices , esp. resistors, capacitors and inductors. For all these devices the use of the existing layers of the core CMOS process (with the potential addition of several technological steps at a reasonable cost) might be an interesting alternative to the integration of these devices on a packaging substrate; since it allows a better form factor and less SMT, though usually at the expense of the obtained performance.

VI.5.a Resistors

Resistors are fairly common features in an IC, though the electrical specifications are usually less stringent than those of discrete devices (accuracy, uniformity, matching, TCR, etc.). Advanced R&D is unlikely in that field.

VI.5.b Capacitors

Owing to the area needed for capacitors, the general trend is to increase the area capacitance of the device, mimicking the previous developments of the DRAM cell. One can think of using standard materials (Al or poly as an electrode and SiO_2 or SiN as an insulator) in a 3D or textured integration scheme. However, the tremendous increase of process complexity (high aspect ratio etching, deposition with excellent step coverage, etc.) and the restriction to low temperature processes along with the limited benefit of this approach push to develop

new materials with a potentially better gain. The introduction of less common materials still needs an important R&D effort: the process is complex, demanding (the introduction of these materials in an interconnect scheme brings specific constraints, e.g. thermal budget, which limits the benefit of these new materials) and the physical and electrical behaviors of these stacks are at present still not fully understood.

VI.5.c Inductors

Obtaining an inductor with a high quality factor above an IC is quite a challenge: due to the long wavelength of the signal at the usual frequency (few GHz translate in mm), the inductor optimization involves not only the design of the inductor itself, but also the underlying layers including the substrate which plays a role in the capacitive and inductive losses.

Technological trends in the development of high performance inductors include:

- thick Cu with a potential routing capability (i.e. with a tight pitch) in and on low k insulators
- magnetic materials to localize the magnetic flux
- patterned metallic layers to shield the inductor from the underlying patterns
- semi-insulating substrates (high resistivity substrates –not readily available for the higher wafer diameters-, silicon on insulating materials, porous silicon, etc.)

On the design side, there is a lack of accurate 3D simulation tools taking in account not only the first order calculation of the inductor itself, but also the long range interaction with the IC.

VI.5.d MEMS

The integration of rf-MEMS potentially allows a simpler redesign of the rf subsystem. Owing to the processing complexity of these devices, it is unlikely for yield reason that mots MEMS devices will be integrated at the wafer level: it is thus expected that the ‘above IC’ approach will be limited to devices whose fabrication only needs few processing steps or mask levels. However, an important R&D effort can be foreseen looking for a simplification of the process, allowing the integration of some micro-systems like micro-switches, variable capacitors and resonators, which will at the same time increase performance compared to the equivalent function with electronic devices.

VI.6. Wafer molding

As the development of microelectronics is still driving towards further miniaturization, flip chip and wafer level redistribution technology (WL-CSP) have been widely accepted as a means for maximum miniaturization with additional advantages. These techniques do generally not include an explicit encapsulation layer, but only die passivation and redistribution layers, respectively. To fulfill the reliability demands of harsh environment applications, the use of an additional encapsulant is crucial. This is especially true for future

applications as high temperature packages or miniaturized SIPs (system in package) and MEMS, where the encapsulant is protecting the sensitive structures generated at wafer level.

To date wafer level encapsulation generally realizes one chip packages of miniaturized outer geometries. Encapsulation functionality is mostly mechanical protection and optical shielding of the active structures. Future development steps of wafer molding will not only integrate single chip modules but also multiple active devices, chip stacks, MEMS and MOEMS. The possible development steps for wafer level SiP encapsulation will evolve from simple protection of the active layer against aggressive media to functional packaging using materials with added functionality allowing the integration of e.g. optical devices as micro lenses or provide shielding and RF functionality by integrated antennas (see **Fig.13**).

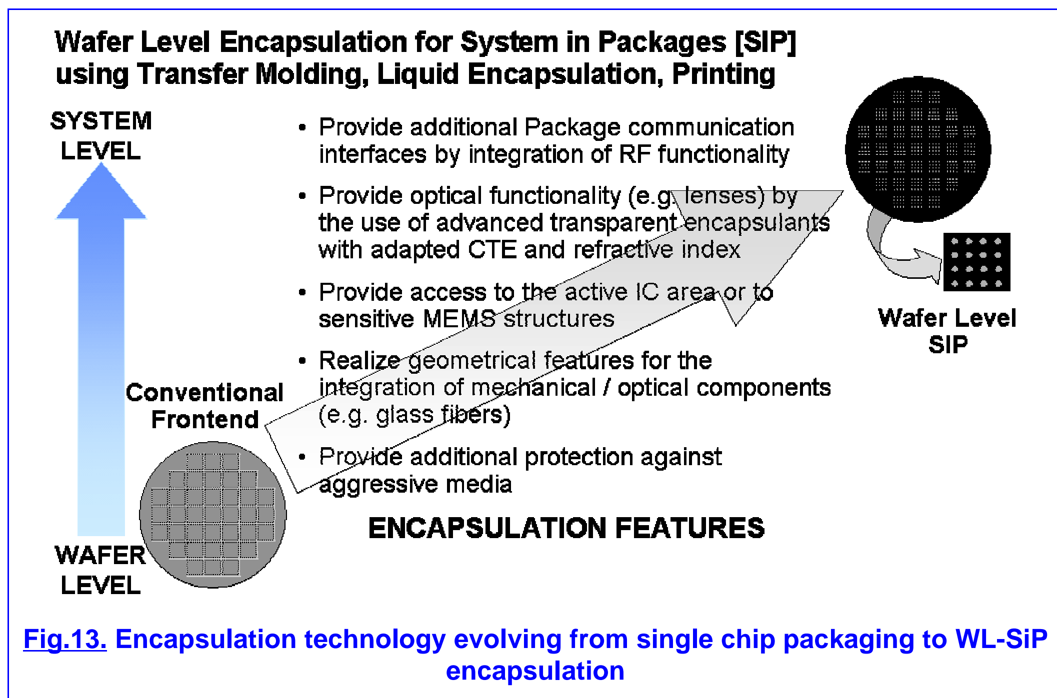


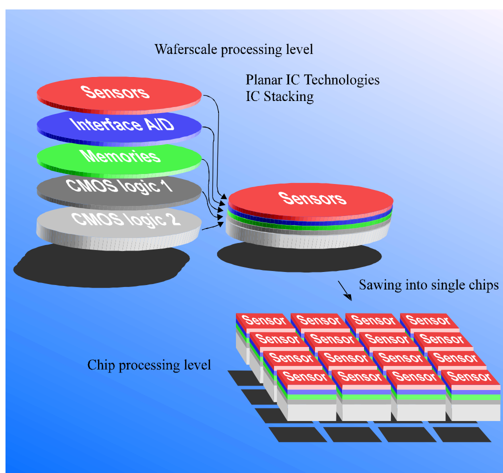
Fig.13. Encapsulation technology evolving from single chip packaging to WL-SiP encapsulation

VII. Vertical System Integration (VSI)

Future microelectronic applications require significantly more complex devices: Besides the trend towards higher integration density there is also a demand for more functionality and increased performance. Due to added device content, chip area will also increase. Performance, multi-functionality and reliability of microelectronic systems will be limited mainly by the wiring between the subsystems (so-called "wiring crisis"). This leads to a critical performance bottleneck for future IC generations. 3D system integration creates a basis to overcome these drawbacks. Furthermore, systems with minimum volume and weight as well as reduced power consumption can be realized for portable applications. Conventional fabrication is based on embedded technologies which are cost intensive. 3D integrated systems show reduced chip areas and enable optimized partitioning, thus decreasing the fabrication cost of the system. An additional benefit is the enabling of minimal interconnection lengths and the elimination of speed-limiting inter-chip interconnects.

3D integrated systems are not a new concept and major R&D programs were developed in the past. However, there are recent breakthroughs in few key technological steps , namely wafer thinning and handling of thin wafers, wafer bonding and through-wafer vias.

A 3D integration method, called InterChip Via technology, based on thinning, adjusted bonding and vertical inter-chip wiring of completely processed wafers has been described and evaluated elsewhere (**Fig.14**). The InterChip Via technology provides very high density vertical interconnects, based on W- or Cu-filled inter-chip vias between metallization levels of thinned device wafers bonded with polyimide as intermediate layer (**Fig.15**). The fully modular concept allows for the formation of multiple device stacks.



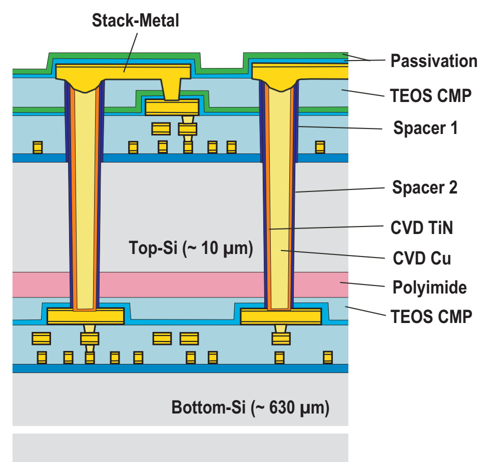


Fig.14. Vertical System Integration	**Fig.15. InterChipVia technology (ICV) – schematic of a vertically integrated device stack**

VIII. System-in-Package

VIII.1. Definition

System-in-package is a packaging concept comprising one- or multiple-chip-solutions which may be combined with other components such as sensors, actuators, passive components or plugs and which are generally housed in a standardized frame. The degree of integration reaches the point where the individual sub-functions will not be operationable without their corresponding parts and the overall function can only be realized as a "joint venture" of all the partial and sub-functions involved (**Fig.16**). Realizing these components in a single element produces a large number of benefits. They have a much smaller, lighter and more robust structure and can be manufactured at a lower cost. For the past couple of years, Japanese companies have been marketing a CSP version of two chips layered on top of each other in a common frame (**Fig.17**). More recently, Sharp has introduced the first package integrating three chips. These have been manufactured mainly from thin silicone wafers using specially modified chip- and wire bonding techniques.

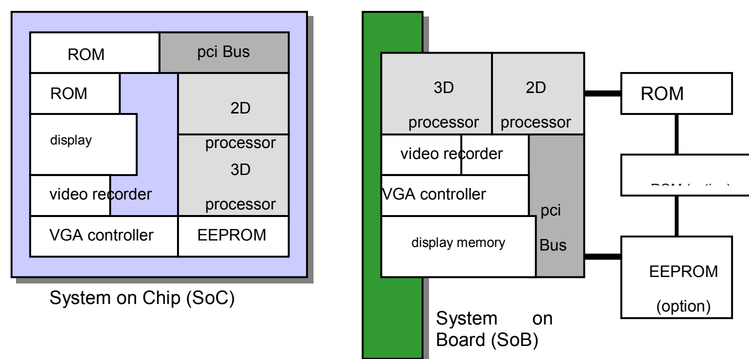


Fig.16. Block diagram of a graphic processor in a system-on-chip-representation and a functional diagram at the board. Both types of design feature combinations of IP-blocks. SoC has the advantages of size and price (for large production lots). The board-version has the advantages of a higher flexibility and the shorter time to market

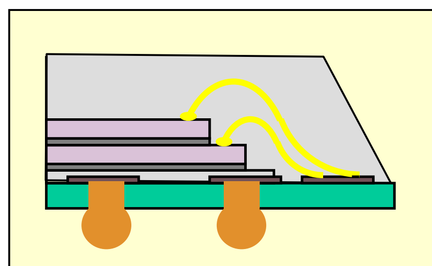


Fig.17. Through the integration of two chips in one package, stacks are lighter than area-array-configurations and need less space

The multichip module (MCM) and its development into complex SiP solutions of maximum functionality have introduced a new level of assembly and bonding technology simplifying the realisation of optimized subsystems. They increase the system performance while at the same time reducing cost and volume. They are also paving the way for the integration of chips from different production technology backgrounds. The idea at the heart of SiP, meanwhile, remains – as explained above – the use of given package geometries and connecting terminals. This may involve leadframe-based or area-array-packages, but also laminated elements such as smart cards or tags with spools for the purpose of communicating with the environment.

We shall now try to show what concrete form such systems may take in the industrial reality, what requirements these package types will be subjected to and where the development trends may lead in the future. We will quote four examples to illustrate the different aspects of the system-in-package.

VIII.2. Micro-mechatronic packages

SiP's mechatronic integrating both actoric and sensoric functions and the electronic data processing (software) in the component itself are characterized by an optimal use of the available space, faster data transmission rates between sensoric and actoric functions and by µ-processors. The packages should have standardized interfaces for their mounting surface and I/O-array, and possibly also an outside geometry adapted to the application, allowing, for instance, the atmosphere to reach the integrated sensor in a pressure sensor or featuring mechanical alignment assistance to facilitate the assembly (**Fig.18**).

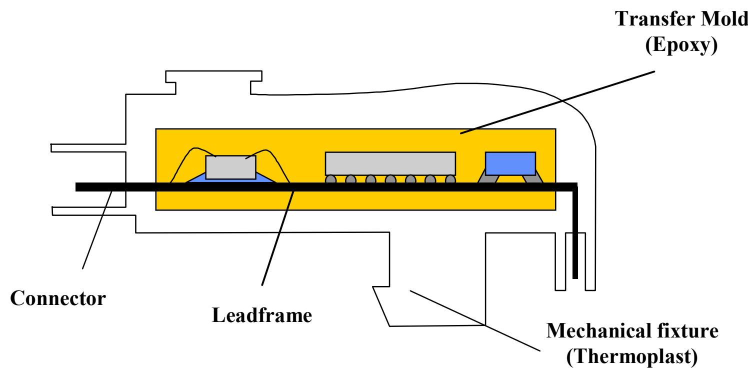


Fig.18. "Clip-On"-connections require the use of thermoplastic materials. Duroplastic materials (epoxide) encapsulate the components. Plug, heat source, mounting clip (thermoplastic)

The conditions under which the sub-modules and the integrated systems are ultimately meant to perform may be extremely rough and may feature high temperatures, toxic fumes, contact with corrosive media etc. Automotive electronics in close vicinity to the engine, for example, are continuously subjected to temperatures in excess of 150°C and to contact with aggressive media. The encapsulation technique of choice for such applications is transfer molding, permitting the manufacture of packages which will be able to withstand atmospheric temperatures of 180°C while maintaining a high degree of reliability. Additional mechanical functionality may be attained by combining this technique with conventional injection-

moulding, enabling the attachment of mechanically strong plug collars and mounting clips right at the package.

VIII.3. Area-array-packages

Unlike MCM's, SiPs go beyond the mere integration of different functions: they pack them into one frame with a standardized contact pattern. Due to the rising lead count, the trend is moving in the direction of area-array contact configurations. These area-array-packages like the ball-grid-array (BGA) or the chip-scale-package (CSP) enable the engineers to place the complete functionality of an entire system on the surface of a (standardized) single-chip-frame. Whereas the BGA – due to the carrier size – represents a fairly relaxed technological environment for the addition of the single components, the smaller (CSP-like) configurations put the bar somewhat higher.

The passive components and IC's integrated into one system may sometimes have differences in dimension to an extent which makes it possible to reduce the entire system to the area surface of its largest component. This, however, requires 3D-integration techniques. Here are some examples for technologies which are already partially used in the manufacturing process:

- Subsystem-forming chips (such as processors, flash memory and SRAM) can be stacked by chip-&-wire-technology and encapsulated in one common frame using advanced wire bonding and encapsulating technologies and new manufacturing techniques. Since the SRAM is larger than the flash and the microprocessor, the two small chips will be mounted (i.e. glued) on the SRAM and subsequently bonded to the substrate carrier. In order to keep the configuration low, these IC's have been thinned to about 70 µm. Alternatively, one may combine flip-chip- and wire bonding techniques in either of two different ways (**Fig.19a**). Both concepts also enable the integration of MEMS-components and passive components.
- The use of flexible substrates which allows the execution of a planar design with existing manufacturing machinery before they increase the degree of miniaturization by folding may also complement the SiP-technology. As an example, we are showing a product from Valtronic, where several chips and peripheral components have been mounted on to a flex-substrate (by flip-chip-technology, a.o.). This is then folded and molded to create a complete system with minimal volume (**Fig.19b**).

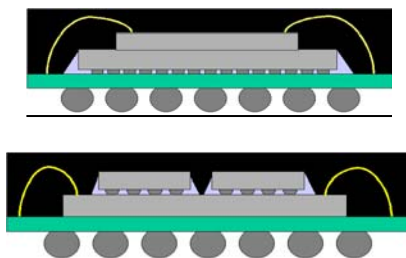


Fig.19a. Two types of stack: flip-chip- and chip&wire-technology

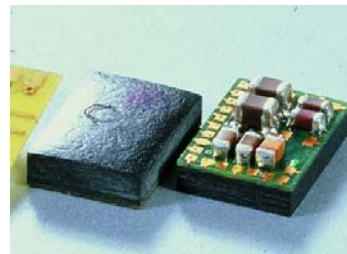


Fig.19b. Module after folding and encapsulating (Source: Valtronic, Switzerland)

VIII.4. Smart-card-packages

A special group of SiPs is not connected to the outside world via permanent electric and mechanic contacts: these are the so-called Smart Cards and Smart Labels. They are connected with read-write-devices via outside contacts (modules) or via electromagnetic fields. Their configurations cover a particularly wide range, reaching from ISO-cards and printed labels via key-chains and coins to glass tubes for the identification of animals. Still, only the Smart Cards contain standardized packages. The essential properties and functions are defined by the ISO-standards of the 7816 series. All label forms have so far been standardized only as far as their communication with the outside world on certain frequencies is concerned; their geometrical design remains free from any rules and regulations (largely due to the communication being wireless).

For all cards without contacts, the basic components are the same: transponder-IC, antenna and possibly some passive elements. The systems, however, may be classified according to the frequency range or their energy supply. There is a distinction to be made between active transponders with their own energy source and passive transponders which must be supplied with energy through an external field.

In order to widen the functionality range of mobile data carriers, other components are increasingly being integrated. The system can be complemented by batteries and additional circuits such as micro controllers and memory elements, but also by foil displays and keyboards, as demonstrated by the examples shown in **Fig.20**.

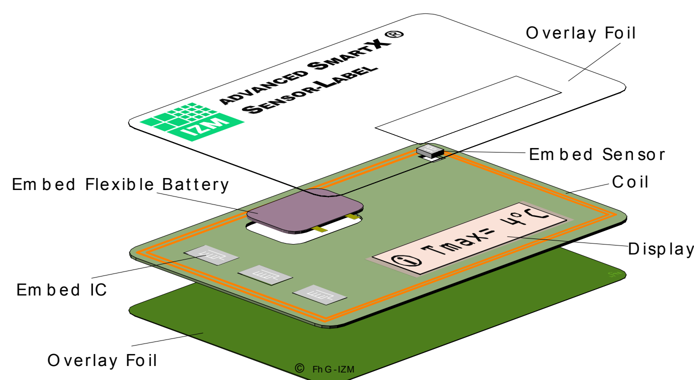


Fig.20. Multifunctional Smart Card with display and battery

The substrate, the mechanical foundation of the system, is most often made from a polymer foil such as polyimide, polyvinyl chloride or polyester, with conductor tracks made from structured Cu or Al or a printed polymer thick-film paste. These substrates make it possible to work with cards and tags of low active height and flexibility. The bonding techniques of choice for the components are normally gluing techniques (due to the temperature sensitivity of the materials involved). For the ICs, techniques on the basis of isotropically and anisotropically conductive adhesives are available. Other components (SMDs, displays, batteries) are mounted with isotropically conductive adhesives. For the purposes of encapsulating such systems, mainly cost-efficient laminating techniques are applied.

VIII.5. System integration in polymeric substrates

Printed circuit boards (PCB) in which components are being developed. Recently, certain multiplayer PWBs that incorporate RCL components (resistors, capacitors and inductors), filters and transformers have been put into practical use in cellular phones. Advance in technical development in the future is expected. In addition, not only passive devices, but also active devices and optical components will be embedded in organic boards. This will open the way to three-dimensional functional modules that represent packaged total systems. An example is shown in **Fig.21a** and **21b**.

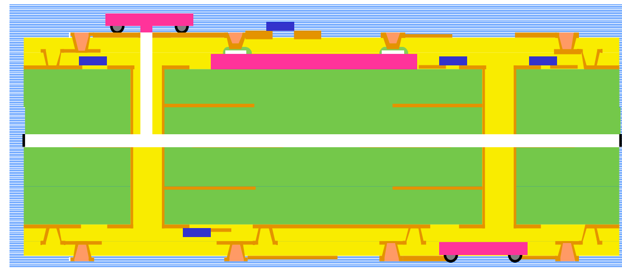


Fig.21a. Embedded ICs, optical components and passives in a motherboard

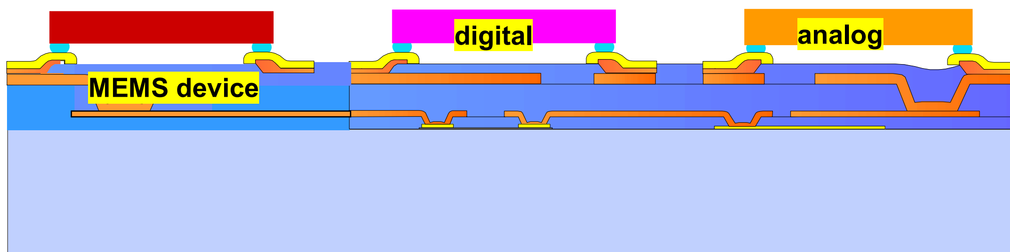


Fig.21b. Hybrid solution: Combination of different ICs on a thin film substrate

VIII.6. Market demands

Existing market uses for SiP include RF and wireless devices, networking and computing, optical systems, mechatronic and MEMS systems and memory applications such as smart or flash cards. SiP technology allows multiple advanced packaging technologies to be combined to create solutions customized to each end application.

There are several reasons why the market demand seems to be growing strongly for SiP solutions.

These include:

- ***Time to market:*** It is often faster to combine ICs in an SiP than it is to implement SoC at the IC level. It is also faster to make changes to the system at the SiP level than to change the entire mask set of an SoC solution. Designing a SoC is a complex, costly and time consuming process.
- ***Size:*** The size of sub-system can be reduced by integrating multiple ICs and other components in a SiP.
- ***Diverse component form factors:*** SiPs can carry flip chips, COB, SMT discretes, sensors and actuators based on the sourcing needs of the application.
- ***Lower system cost:*** An optimized SiP solution usually results in an overall system cost reduction compared to discrete IC packages.
- ***Electrical characteristics:*** Performance is enhanced through shorter interconnections between ICs in a SiP; e.g. by placing the logic and memory chips close to one another for memory data speed enhancement.
- ***Thermal management:*** Often, common heat sinking approaches can be used with SiPs to minimize the number and handling of individual thermal solutions.

IX. R&D requirements for advanced system packaging

The integration of chip technologies and packaging for building a true System in a Package needs developments in many directions:

- chip and package should be co-designed in order to optimize the overall size, performance and cost of the system. For this goal, extended material and process characterization will be needed in order to provide accurate mechanical, thermal and electrical models for this overall optimization. More specifically:
  - a mixed signal co-design and simulation environment should allow to deal with the different scales of the devices themselves (e.g. IC blocks) and the whole system (e.g. substrate)
  - better analysis tools have to be developed for transient thermal effects and integrated thermo-mechanical behavior
  - especially with the increased frequency/ current of the future systems along with the lower voltage switching and associated noise margin, efficient electrical tools should tackle power disturbances, signal integrity and EMI issues
- advanced CMOS processes will induce specific problems in packaging owing to the reduced mechanical stability and heat conductivity of the Cu/low k interconnection system: direct wire bonding or bumping to Cu, bump and underfill optimization for insuring low k and interfaces integrity are key words of these needed developments
- the integration of RF components either on a chip or in a substrate for the transducer nodes of a distributed intelligence system. Strong R&D is needed for introducing new materials and wafer level technologies especially for capacitors, inductors and mechanical devices (resonators, filters, switches, etc.)
- for internal communication in the integrated system or for fixed systems optical component integration will be a key topic which is not addressed in the present report
- owing to the limited pitch of the PCB, techniques for increasing the pin count for a given foot print will be a key driver: area array packaging (flip chip, CSP, system-CSP) has thus to be developed preferably with wafer level techniques in order to reduce the cost per die. In this respect:
  - fine pitch and multilayer technology will reduce the gap between die pitch and board pitch
  - cost-efficient bumping will allow the generalization of area array packaging. Change in materials, esp. the suppression of lead for

environmental and soft error issues, is a definite challenge, along with the thermal cycling, testing and reparability

  - o bumpless and thin interconnect layers e.g. thin barrier and active solder layers, will be required for thinned silicon devices and flexible substrates, or 3 D system integration

- the trend towards flexible portable distributed systems will translate into reliable flexible substrate materials compatible with the size and properties of the devices to be integrated

- in order to accommodate the cost requirement, wafer level integration will be a major direction for R&D. However:

  - o wafer-to-wafer integration is expected to prevail for high yield processes of wafers with similar size

  - o the heterogeneity of devices to be integrated (different wafer sizes, low yield, etc.) will push the die-to-wafer approach

  - o in any case the thinning of chips and wafers and their handling will be key techniques for mastering a true 3D integration

- more pressure will be applied for a better environmentally compatible manufacturing

INTEGRATED ENERGY SUPPLY

Robert Hahn and Hugo de Man

Several segments of the portable market have annual growth rates of up to 50 %. Thus the number of electronic appliances is dramatically growing which increases the importance of their power sources as well as their environmental impact. For devices, which are distributed in the user's local environment, handling extended functionalities and enabling ambient intelligence implementation through an active tagging technology, size and cost of most active tags are more or less dominated by the power sources.

These autonomous systems require energy coming from a miniaturized power supply. It translates into a higher demand on an efficient energy generation or conversion and/or an increased energy density of the energy storage system. Since batteries have a low potential for high energy density and low weight, innovative solutions have to be worked out.

In the case of a body area network, harnessing energy from the human body seems the most appropriate solution. On the other hand, for the distributed networks of transducer nodes, one has to provide an energy supply for an extended period of time and in some case for the whole system lifetime (typically many years): miniaturized fuel cells, micro-solar or light modules and the energy in vibrations from the outside world (e.g; walls,…) are attractive solutions.

Energy supply for future electronic products is not an added, discrete feature but a system functionality which has to be fully integrated in the system development. It requires alliances of developers, manufacturers and end user groups.

I. Harnessing energy from the human body

The human body is a storehouse of energy. Body heat, body motions (breathing, walking,…) and in the future biochemical energy stored in body fluids can be converted into electrical energy. The conversion of body heat and of kinetic energy seems the most attractive short term. In the latter case many solutions exist in the macroscopic world and could be translated as micro-systems: the use of a variable capacitor with a fixed charge between the capacitor plates is a promising example, shown in **Fig.22**.

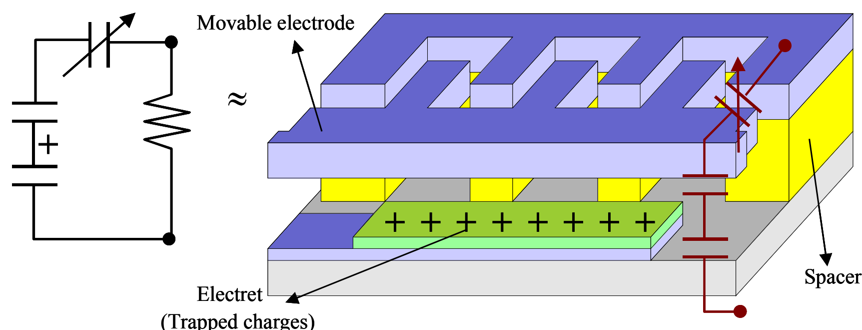


Fig.22. Energy harvesting from motion

The design of such power sources will be of crucial importance for the further miniaturization of body area networks.

II. Energy sources for distributed networks of transducer nodes

II.1. Long lasting energy source

Batteries, and more recently micro-fuel-cells, are key candidates for providing energy to an autonomous system for a short period of time.

Micro-fuel cell development is based on thin film and micro patterning technology (MEMS). Wafer level and foil processes which are used for high density interconnect electronic modules and wafer level packaging have been adapted to micro fuel cell development. Planar cells of the size between 1 mm^2 and approximately 1 cm^2 will enable the fabrication of energy sources in application fields of small portable devices, replacing thin Li-polymer batteries, button cells or zinc-air batteries. The required miniaturization and cost reduction is achieved by the use of planar micro patterning technologies.

Serial interconnection of individual cells is attained with gang bonding technologies. A dispensing technique or screen printing is used for integrated planar sealing. The system is mechanically flexible for easy integration into the surface of electronic devices and low volume consumption. The anode micro flow field has been patterned with dimensions down to 10 µm.

Today hydrogen storage or generation is not applicable to miniaturized and portable systems. An energy density advantage of factor 2 to 5 over Li-Batteries can be achieved with methanol. Therefore further investigations are focusing on direct methanol fuel cells (DMFC).

Along the same line, potential new approaches may emerge in the future like the micro-turbine development at MIT.

II.2. System lifetime lasting energy source

The concept of a one-time energy supply implemented in the system during its fabrication and providing enough energy for reliable operation during the entire system lifetime seems very attractive. Given the constraints in terms of volume (a few mm^3) there are many possible solutions: batteries and chemical energy, nuclear energy, mechanical energy and photo-generators.

Batteries do not, even with state of the art technology, meet the density requirements needed to provide 100 µW during several years. Chemical energy as available in thin film fuel cells, could be a viable option although a lot of research still needs to be done in this field. In any case, these solutions will have a limited lifetime.

Although nuclear energy yields the highest density it can be expected that that energy source in micro scale applications will be probably of limited use and limited to very specific applications.

The system could also take the energy from vibrations of the outside world (e.g. walls): this is basically the same concept as the kinetic energy acquisition from the body, though usually with a much smaller power and/or intermittent energy supply, limiting its use.

Solar (or light) energy is the most attractive solution. However, its application is limited by the fact that the system need access to some light source and that energy storage has to be added for intermittent illumination of the device or for accommodating energy surge in the system.

III. R&D requirements in energy subsystems

Beside the general trend of reducing the power consumption of the electronics, specific developments are needed in the field of energy subsystems:

- true integration of the energy part into the **design flow** of the heterogeneous system. Of special importance is the optimization of power management system to improve performance and lifetime of the power sources at a much lower cost for smaller handheld products. For each kind of power source, this in turn put emphasis on:
  - hardware/ software co-design in order to take benefit of the specific behavior of the chosen power source (energy, voltage stability, surge current,…)
  - integration of dedicated technologies for converters and regulators, e.g. development of novel integrated power inductances for very low profile DC-DC converters and cell balancing systems of small battery packs
- true integration of the energy part into the **fabrication** of the heterogeneous system:
  - miniaturization of long lasting energy sources: size and form factors, encapsulation, use of thin and adaptable polymer technologies, increase of energy density.
  - use of chip scale packages and low cost processes for power sources and power electronics
  - development of wafer level processes for micro power sources
  - take into account specific reliability patterns
- development, integration and thermal management of **micro fuel cells** as alternative energy source for portable electronics, esp. direct methanol fuel cells
- development of new technologies for miniaturized **solar modules** with high efficiency and the option of being mechanically flexible
- future visions of mobile electronics are comprise concepts like wearable computing, ubiquitous computing, body area network and others which have special power needs. It translate into the development of **mechanically flexible power sources** for e.g. clothes and into the management of **area distributed energy sources**
- primary and secondary batteries of portable systems are responsible for the major share of heavy metal pollution in domestic waste and lead to a damage to the environment and human health. The **environmental aspects** of integrated power sources have to be built in the developed solutions.

Figure captions

Fig.1. Heterogeneity as a general trend

Fig.2. Integration of heterogeneous components with advanced substrate or package in a system

Fig.3. Bringing different IC's and passive components in a single integrated system
(from: http://www.amkor.com/enablingtechnologies/SIP/)

Fig.4. Stacking different components in a single integrated system (two types of stack: flip-chip and chip & wire technologies)

Fig.5. HP ink jet cartridge as an example of MEMS (or micro-mechatronic) package

Fig.6. Microphone and ASIC chip on Cu leadframe
(from: http://www.cdnet.edu.cn/mirror/singap_college/www.ime.org.sg/adv/adv_mems.htm)

Fig.7. Multifunctional Smart Card with display and battery

Fig.8. Ambient Intelligence System

Fig.9. The design gaps

Fig.10. The 'total' design approach

Fig.11. A vertical approach for collaborative research in heterogeneous system design through Focus Centres of Excellence

Fig.12. An integrated approach of manufacturing testing of heterogeneous integrated systems

Fig.13. Encapsulation technology evolving from single chip packaging to WL-SiP encapsulation

Fig.14. Vertical System Integration

Fig.15. InterChipVia technology (ICV) –schematic of a vertically integrated device stack

Fig.16. Block diagram of a graphic processor in a system-on-chip-representation and a functional diagram at the board. Both types of design feature combinations of IP-blocks. SoC has the advantages of size and price (for large production lots). The board-version has the advantages of a higher flexibility and the shorter time to market

Fig.17. Through the integration of two chips in one package, stacks are lighter than area-array-configurations and need less space

Fig.18. "Clip-On"-connections require the use of thermoplastic materials. Duroplastic materials (epoxide) encapsulate the components. Plug, heat source, mounting clip (thermoplastic)

Fig.19a. Two types of stack: flip-chip- and chip&wire-technology

Fig.19b. Module after folding and encapsulating (Source: Valtronic, Switzerland)

Fig.20. Multifunctional Smart Card with display and battery

Fig.21a. Embedded ICs, optical components and passives in a motherboard

Fig.21b. Hybrid solution: Combination of different ICs on a thin film substrate

Fig.22. Energy harvesting from motion

Table captions

Table 1. WL-CSP Technology Alternatives. Sources: Prismark and TechSearch

Glossary

Ambient Intelligence distributed intelligence through integrated smart systems which are conscious of and self-adapting to their environment while communicating with a dynamically reconfigurable network of other devices

AmI *see* Ambient Intelligence

ATE *stands for* Automatic Test Equipments

ATPG *stands for* Automatic Test Pattern Generator

BAN *stands for* Body Area Network

CAE *stands for* Computer Aided Engineering

Chip Scale Package package whose size is roughly the size of the chip

Chip Size Package package whose size is exactly the size of the chip itself

COB *stands for* Chip On Board

CSP *see* Chip Scale Package or Chip Size Package

DfT *stands for* Design for Testability

DRAM Dynamic Random Access Memory: 'low cost' high density memory which has the capability to store and read a large amount of data with a low cycle time, but at the expense of a periodic refresh of the data. A specific technology is needed for obtaining the high density, inducing an important added cost for embedded memories.

DMFC *stands for* Direct Methanol Fuel Cell

DSM *stands for* Deep SubMicron technology

EDA *stands for* Electronic Design Automation

Encapsulant mechanically and optically protective layer of the sensitive structures generated at wafer level

FBGA *stands for* Fine pitch Ball Grid Array

FCB *see* Flip-Chip Bonding

Flip-chip Bonding Technique where bumps (solder balls) are grown over the pads of the die and the chip is flipped on the PCB for connection

FRAM Ferroelectric Random Access Memory: memory having the potential to replace DRAM, SRAM and NVM, though having a limited cyclability

ITRS International Technology Roadmap for Semiconductors, which describes the needed developments in the different fields in order to stick with Moore's law in the next decade

MCM *stands for* Multi-Chips Module

MEMS Micro-Electro-Mechanical System: miniaturized electronic device having a moving part translating mechanical into electrical signal or vice versa

MRAM Magnetic Random Access Memory: memory having the potential to replace DRAM, SRAM and NVM

NVM Non Volatile Memory: 'medium density' memory which doesn't need power supply to maintain the stored data, but have a limited capacity of cycling. Many different types of NVM exist and the added processing steps add a significant cost in ICs with embedded memories.

PCB *stands for* Printed Circuit Board

Printed Wiring Board multilayer substrate

PWB *stands for* Printed Wiring Board

QoS Quality of Service

rf *stand for* radio-frequency

SMT *stand for* Surface Mount Technology

SiP *stand for* System in a Package

SoC *stand for* System on a Chip

SoP *stand for* System on a Package (see System in a Package)

SRAM Static Random Access Memory: 'high cost' high speed memory with medium storage density; power supply is needed to maintain the information. The technology is compatible with a standard CMOS process.

System in a Package packaging concept comprising one- or multiple-chip-solutions which may be combined with other components such as sensors, actuators, passive components or plugs and which are generally housed in a standardized frame

System on a Chip system's functions implemented on a single chip

Underfill(ing) material inserted between the chip and the board in order to accommodate their mechanical mismatch and avoid reliability issues

Wafer Level Packaging technology in which all of the IC packaging is performed at the wafer level. In this technology, the cost per die is a function of the wafer processing cost and no longer proportional to the number of I/Os. The number of I/Os is limited by the wiring density at the board level.

WBAN *stands for* Wireless Body Area Network

WLAN *stands for* Wireless Local Area Network

Comments from external experts

The content of the draft report was presented to different experts, including the **MEDEA+ staff** and the **MEDEA+ Board Support Group**. The following comments were made for an improved version of this document:

- the document should list in an Appendix the on-going and past projects related to the proposed research areas
- it should bring some insight as to how the choice is made between an SoC and SiP approach (or any in-between solution)

On the other hand, it was stressed that this document:

- doesn't specifically address the applications needing integrated heterogeneous systems (however this report is expected to fit the MEDEA+ Application Roadmap)
- is not a market analysis
- doesn't provide a technology roadmap
- is not a benchmark of the excellence of the research teams within Europe
- doesn't propose specific research projects to be started, but merely outline future directions of R&D in the field of heterogeneous systems

Some more comments came from the discussion between the panelists and the audience at a **Workshop** held on **June, 4 in Leuven**. Generally speaking there is no general rule for choosing between SoC and SiP: at a given point in time for a given function, SiP may allow an early market entrance of a product using widely different technologies, while at a later time the same product line may move to an SoC approach for higher volume or to an higher complexity with a combination of SoC + SiP approach (s. **Fig.A1**).

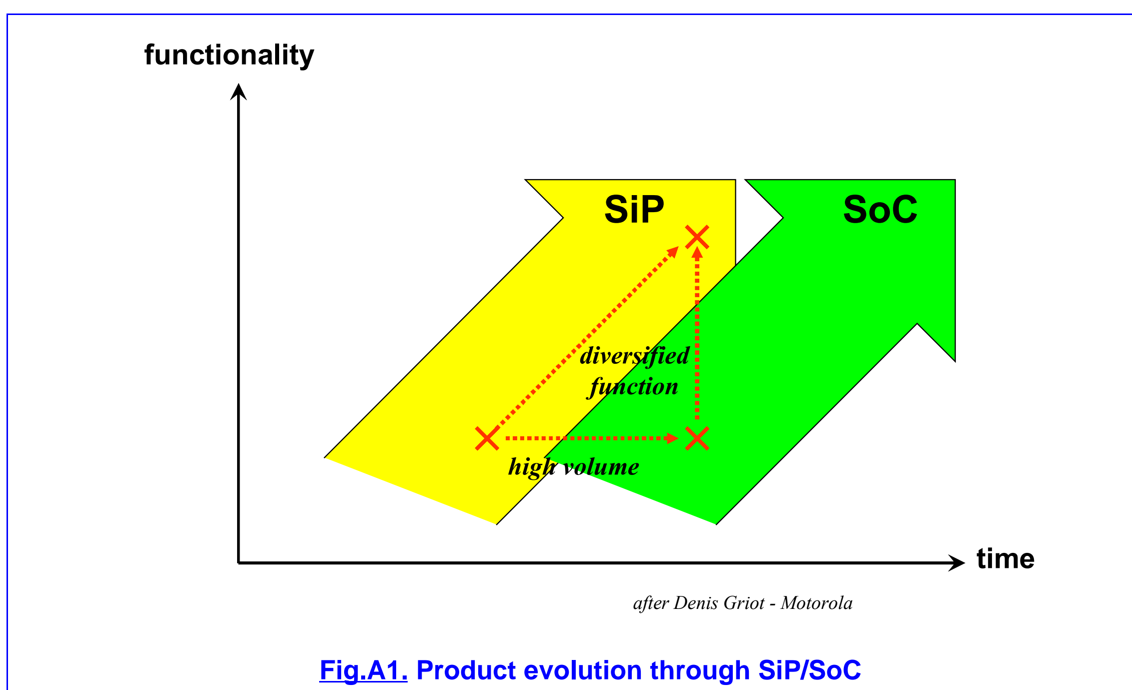


Fig.A1. Product evolution through SiP/SoC

From the past experience (CMOS vs. nMOS, BiCMOS, etc.), the integration of very different technologies on a single chip will prevail ("If SoC is feasible, then SoC is the winner") even with an apparent increase in cost/ mask count.

More specifically, in the field of design:

- there is a confusion between tools and methodology. What we need is an application-specific design methodology that can help in solving the problems of system level design.
- there is no need for a separate full CAD frame development in Europe (an attempt has been done in the past in JESSI, but it failed, due to lack of market in Europe): only specific missing tools should be developed in Europe, when big US companies are not interested in offering solutions
- only 50% of expected design efficiency can come from standard tools. Design methodology is important: once a solution has been defined, smart people will be able to make a business out of it
- reconfigurable systems, based on software are very expensive in terms of power. Most of the power saving can be done at architectural level, optimizing memory access (as stressed in the report, e.g. in III.2.a).
- most of the problems come from the fact that software developers, designers and technologists talk different languages and do not understand each other (s.III and IV in the report for the need of a collaborative research bringing together experts from different fields).

A very important comment was the following: presently, the system design methodology exists in Europe, not in semiconductor companies but in system houses. However the system houses are getting out of system design to move into the service business, and there is a risk that the necessary link between systems – IC – technology and the associated knowledge will be lost.

Regarding the technology aspect:

- for the next years, device scaling will still be the primary driving force in Microelectronics.
- mask count is important, but also technology complexity
- SiP must be only used for functions which can't be implemented in time through existing processes or through software
- from a practical aspect a direct combination of complex chips in a SiP is not possible, unless by using an interposer (re-routing). Presently it is difficult to ensure that the bumps/ pads layout will be stable over months when the chips are produced elsewhere.
- integration of power sources is not motivated (only) by costs, but also by security (e.g. smart cards). They are not necessarily batteries but could be power sources.

Other points were raised:

- reliability of new technologies for automotive applications is not emphasized
- there is a lack of support to design research in Framework 6
- small companies have no access to advanced silicon technology