Master Thesis/Internship

2015 Topic Guide
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Students from universities and engineering schools can apply for a Master thesis and/or internship project at imec. Imec offers topics in engineering and (industrial) sciences in different fields of research.

All Master internship and thesis projects currently available at imec are collected in this topic guide. The projects are classified according to the imec research domains. You can find more detailed information on each research domain under the heading ‘R&D Offering’ on www.imec.be.

How to apply?

Send an application e-mail including your motivation letter and detailed resume to the responsible scientist(s) mentioned at the bottom of the topic description you choose. The scientist(s) will screen your application and let you know whether or not you are selected for a project at imec. It is not recommended to apply for more than three topics.

There is no application deadline. We accept applications at any time and deal with them throughout the year.

Master internship students usually receive an allowance. However, some research groups only accept self-supporting students. Do you want to know upfront whether the project you wish to apply for provides financial support? When sending in your application e-mail check the remuneration details with the responsible scientist.

For more information, go to the Internship and Master Thesis page under the heading Education on our website. Do you have additional questions, then send an e-mail to student@imec.be.
I. CMOS Scaling

First principles filament size and stability in CBRAM devices

With the continuously changing landscape of the computer technologies, a new memory type is needed that will be fast, energy efficient and long-lasting. It shall combine the speed of RAM and be non-volatile in the same time. Resistive RAM (RRAM) or more specifically the Conductive-Bridge RAM is one of the most promising candidates in this respect. The CBRAM device is formed of a Cu filament in an insulating matrix (am-AI2O3, am-SiOx, etc.). The available atomistic simulation tools can help us to understand the CBRAM filament at the atomic level: investigate the Cu cluster size stability, simulate its electronic and electrical properties that will be cross-referenced with the experimental measurements. Simulated thermodynamic data on Cu cluster nucleation can provide with insight on the filament stability and device switching kinetics.

Type of project: Thesis project

Degree: Master in Sciences or Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering

Responsible scientist(s): For further information or for application, please contact Sergiu Clima (sergiu.clima@imec.be), Ludovic Goux (ludovic.goux@imec.be) and Michel Houssa (michel.houssa@fys.kuleuven.be).
Microbumps cleaning and passivation options for 3D applications

In order to increase the density of memory chips and improve the performance of logic devices besides scaling electronics devices, 3D integration is also necessary. Microbumps are interconnects between two stacked chips to make connection between them. Increasing density of interconnects or reducing pitch of microbumps in 3D integration to improve the performance of final product, requires new UBM (under bump metallurgies) materials and solder, cleaning and passivation options. Master student will study cleaning and passivation of different UBM materials, capping layers and their influence on IMC formation (intermetallic compounds) through papers and experimental results. Parallel to blanket study of capping layers by means of XPS, AFM, Contact angle, ... stacked chips will be analyzed using cross section, SEM and EDS analysis. Results will be presented in IMEC PTW weeks and then external conferences or journals.

Type of project: Thesis project

Degree: Master in Sciences or Master in Engineering majoring in chemistry, materials engineering, electrotechnics/electrical engineering

Responsible scientist:
For further information or for application, please contact Jaber Derakhshandeh (Jaber.derakhshandeh@imec.be) and Kenneth June Rebibis (Kenneth.June.Rebibis@imec.be).

Study IMC formation of different UBM materials with Sn based solders for 3D applications

In order to increase the density of memory chips and improve the performance of logic devices besides scaling electronics devices, 3D integration is also necessary. Microbumps are interconnects between two stacked chips to make connection between them. Increasing density of interconnects or reducing pitch of microbumps in 3D integration to improve the performance of final product, requires new UBM (under bump metallurgies) materials and solder. Master student will study properties of different IMCs (intermetallic compounds) through papers and experimental results. IMC growth rate will be extracted for as plated layers and stacked layers using cross section, SEM, EBSD and EDS analysis. Results will be presented in IMEC PTW weeks and then external conferences or journals.

Type of project: Thesis project

Degree: Master in Sciences or Master in Engineering majoring in materials engineering, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Jaber Derakhshandeh (Jaber.derakhshandeh@imec.be) and Kenneth June Rebibis (Kenneth.June.Rebibis@imec.be).
Investigation of electrical properties of leading-edge scaled CBRAM devices using novel materials for future memory technologies

These last years, the demand for high-density non-volatile memories has been steadily increasing, particularly due to the boom of mobile applications. Key properties that future memories will have to exhibit are high scalability below 10nm feature size, low-current operation, together with write endurance and non-volatility. Today, the Flash technology dominates the market, however will face severe scaling limitations in next technology nodes. To the contrary, the resistive-switching RAM (RRAM) technology is an emerging class of memories that draws more and more attention due to considerable progress in terms of scalability, memory performances and reliability [1]. Between the different RRAM flavors, the conductive-bridging RAM (CBRAM) technology is currently sticking out due to improved performances, not only for low current applications [2], but also for reconfigurable logic circuits [3], or analog applications [4]. On the other hand, excellent reliability improvements were also achieved [5], so that today CBRAM is seen as a major contender for future memory replacement. CBRAM cells typically consist of an insulator material sandwiched between an electrochemically active electrode (typically Cu) and an inert electrodes (typically W), whose processing is compatible with the Complementary Metal-Oxide-Semiconductor (CMOS) technology. Traditional insulator materials are chalcogenides [4], however promising results were recently reported using CMOS-friendly oxides [2,5-7] prepared as very thin layers by advanced techniques. The operation principle of resistive switching relies on the voltage-induced electrochemical oxidation of Cu from the active electrode, followed by the drift of Cu cations through the insulator and reduction into a conductive nanofilament of Cu bridging the two electrodes and turning thus the device into a low-resistive state (LRS). The opposite voltage polarity allows to reverse the mechanism and thus to reversibly turn the device back to a high-resistive state (HRS). The microscopic physics at work during electrical programming of LRS and HRS states is today subject to intense investigation because a more accurate understanding of the switching mechanism will be key for further development of the CBRAM technology. Imec has recently demonstrated leading-edge achievements of integrated CBRAM devices, not only in terms of memory properties [6,7], but also in terms of understanding of the physics at work at the nanoscale during switching [8].

In the framework of a Master-internship research activity, novel insulator- and electrode-material combinations will be investigated to further optimize memory performances, and will be implemented into integration structures enabling possible breakthroughs in terms of technology scaling. These ambitious objectives of identifying material stacks allowing both a better understanding of the switching mechanism and enhanced performances of scaled CBRAM cell will require broad scientific competences, i.e. in the fields of the material physics, material engineering, device physics, and electrical characterization. The work will mainly consist in the electrical characterization of integrated devices, focusing on the investigation of the effects of the processing, the material properties, and the integration steps on the electrical properties of the cell. This activity will involve various measurement techniques (current-voltage, capacitance-voltage, pulse-programming,...). The work will be carried out in the frame of the Imec Industrial Affiliation Program (IIAP), thus in close relation with industrial partners and within a team consisting of experts in various fields.


Type of project: Thesis with internship project

Degree: Master in Sciences or Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Ludovic Goux (gouxl@imec.be).
Microelectronics has revolutionized our technological society. Electronic products in the form of home entertainment equipment, mobile electronic devices, desktop personal computers, and large supercomputers are pervasive in our everyday world. The electronics revolution began in the 1960s with the fabrication of the first integrated circuits (ICs). Since then, this industry has experienced remarkable growth resulting in significantly more complex ICs which are faster and smaller. Conductors, semiconductors and insulators materials are essential to integrated circuit processing. The active device components are composed of semiconductors. Conductors are extensively used for interconnection applications, for electrostatic discharge (ESD) protection of ICs, and for electromagnetic interference (EMI) shielding of electronic equipment.

Insulators, most commonly polymers, are widely used as inter level dielectrics, encapsulates, underfills and materials for the packaging and housing of electronic equipment, and it is extremely important to know their mechanical properties and behavior in order to avoid that they affect the functionality of a semiconductor device. Polymers used in micro-electronics industry can behave as elastic, plastic or viscoelastic material depending on their application. One common use of a viscoelastic polymer is as underfill. This underfill fills the gap between chips (in case of 3D technology) or between the chip and board (PCB) and surrounds the interconnect joints, see figure below.

The purpose of underfills is to protect the interconnect joints from stress and deformation that can occur during temperature variations. However the underfill polymer has a much higher coefficient of thermal expansion (CTE) than the chip and consequently induces high thermal stresses in the chip as a result of CTE mismatch between them. These stresses can damage the chip devices.

One important parameter which should be known in order to avoid the stress is the viscoelastic behavior of these material during processes in which the device is submitted to different temperature profiles. The objective of this thesis is to study the mechanical properties of a viscoelastic polymer at different conditions using different experimental techniques. In the first part of this work the student will explore the techniques that are available for this purpose and benchmark them. In a second phase the student will apply one or more experimental technique using equipment that is available in imec or at the KU Leuven, and extract the mechanical properties as function of temperature and time of a viscoelastic polymer used in microelectronics. The results obtained using different techniques, and the techniques themselves, should be analyzed critically. Samples will be provide by imec.

Type of project: Thesis project

Degree: Master in Sciences or Master in Engineering majoring in materials engineering, mechanical engineering

Responsible scientist(s):
For further information or for application, please contact Melina Lofrano (Melina.Lofrano@imec.be).
Nano-mechanical computational modelling for microelectronics applications

For the past decades, the performance of microelectronic devices has been improved by the semiconductor industry through continuous increase of transistor density which necessitates downscaling of the size of various chip components and also devices required in the fabrication processes. As such, many materials currently used in the semiconductor industry have feature sizes in the nano-meter range which constitutes a serious challenges from a mechanical design and analysis perspective. This has motivated application of mechanical engineering approaches to mitigate mechanical reliability challenges associated with such small sizes in microelectronics including computational modelling methods. In this context, the finite element method (FEM) is widely employed as a powerful tool for mechanical analysis in the reliability and modelling group (REMO) of imec.

In this project the Master thesis student will work within the computational modelling team to develop mechanical computational models using FEM to analyze nano-meter scale membranes and wires of different materials such as ceramics, metals and carbon nano-sheets. The student will verify the computational simulation results by comparison to experimental mechanical test results which will be obtained by novel methods such as nano-indentation, Raman spectroscopy and laser Doppler vibro-meter. The experimental data for model corroboration will be provided by the experimental team members.

**Type of project:** Thesis project

**Degree:** Master in Sciences or Master in Engineering majoring in materials engineering

**Responsible scientist(s):**
For further information or for application, please contact Houman Zahedmanesh (houman.zahedmanesh@imec.be) and Mario Gonzalez (mario.gonzalez@imec.be).
Evaluation of advanced organosilica low-k dielectrics

The constantly increasing density of transistors on a chip enabled by down-scaling of their dimensions led to the situation when the overall performance of the integrated circuit is determined by the latency of signal propagation through the interconnects – multi-layer wiring system linking transistors and various functional blocks. One way to reduce the signal propagation delay is to mitigate the capacitive coupling between the wires by introduction of insulating materials with lower dielectric constant. As a result, traditionally used silicon dioxide with dielectric constant around 4 was replaced by porous silica-based materials containing low polarizable organic groups. Today low-k materials with dielectric constant of 2.5 are already in production while search for material options for future technology nodes is still a field of active study. The candidate will be involved in development and evaluation of advanced spin-on organosilica based materials targeting the range of dielectric constants 2.0–2.3.

One of the possible candidates is a new type of self-assembled organosilicate-based materials prepared by spin-coating of a mixture containing both organosilica precursors and sacrificial organic phase. Assembled upon evaporation the sacrificial template is removed by successive thermal treatment thus producing porous organosilica layer with dielectric constant controlled by the template loading and composition of the organosilica matrix. UV photochemical fragmentation of template molecules will also be studied. The deposited films will be characterized by using advanced experimental techniques like FTIR, XPS, TOF SIMS, ellipsometric porosimetry, nanoidentation etc. Apart from characterization of the films produced from various sol formulations, different strategies of the template removal will be examined as well to find a trade-off between chemical and mechanical stability of the produced films. The generated results are important for future technology nodes of nanoelectronics and will reported during the internal imec meeting, international conference and published in international journals.

Type of project: Thesis with internship project

Degree: Master in Sciences or Master in Engineering majoring in physics, chemistry, materials engineering

Responsible scientist(s):
For further information or for application, please contact Mikhail Baklanov (baklanov@imec.be) and Mikhail Krishtab (krishtab@imec.be).

Evaluation of metal-organic frameworks as low-k candidates for 5 and 3 nm technology nodes

The 5 and 3 nm technology nodes request exploration of new approaches in the device fabrication and integration. In the case of interconnects, it is becoming clear that replacement of damascene technology to “subtractive” approach by metal patterning is requested. The metal patterning allows exploration of completely new types of dielectric materials because similarity to SiO2, which was the key advantage of OSG types of low-k dielectrics, is becoming not important anymore.

One class of new materials that has already been reported as a possible candidate for low-k application is metal-organic framework (MOFs) formed by self-assembling chemistry. These materials demonstrate properties interesting for BEOL technology as have been demonstrated in several recent papers.

We achieved quite interesting results using ab initio calculations of different metal-organic framework. It was found that the metal ions may have the key contribution into ionic polarization and static dielectric constant. Therefore the careful selection of chemical composition is very important. It is more challenging to carry out experimental study. Most of blanked MOF films have significant surface roughness after crystallization and it makes difficult accurate measurement of dielectric characteristics. On the other hand, in the subtractive approach, MOF should be deposited in metal trenches.
Deposition, optimization and evaluation of blanked MOF films as well as deposited inside trenches is the main topic of MS student activity together with PhD student Mikhail Krishtab and collaborators from KU Leuven.

**Type of project:** Thesis with internship project

**Degree:** Master in Sciences or Master in Engineering majoring in physics, chemistry, materials engineering

**Responsible scientist(s):**
For further information or for application, please contact Mikhail Baklanov (baklanov@imec.be) and Mikhail Krishtab (krishtab@imec.be).

Electrical characterization of advanced fully-depleted devices integrated using a monolithic 3D approach

CMOS scaling is facing multiple challenge. The increase in interconnects delays is one of them. As transistors improve with scaling, interconnect delays get worse. The use of repeaters is an expensive solution as it requires additional power and circuit area. 3D integration, which consists in stacking multiple layers of transistors in the vertical direction, allows for shorter wires and therefore reduces interconnect delays, while further increasing the circuit density.

3D sequential integration, also called monolithic 3D integration, by opposition to parallel (or TSV 3D integration) is the only technological option which fully benefits from the third dimension potential at the transistor scale thanks to its high alignment precision compared to TSV 3D. However, the sequential processing of the top transistor can have a detrimental effect on the bottom circuits or devices. Typically, the top transistor needs to be processed at a low thermal budget compatible with the bottom devices, while maintaining good device performance.

Advanced devices based on low thermal budget processing using thin film fully depleted technology such as finFETs or FDSOI devices are considered for this project.

In this work, the candidate will focus on the electrical characterization of device/circuits of the bottom and top layers. He will assess the impact of the top processing on the performance of the devices in the bottom layer. He will also evaluate the impact of different low thermal budget processing options on the top device performance.

**Type of project:** Thesis project

**Degree:** Master in Engineering majoring in electrotechnics/electrical engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Anne Vandooren (Anne.vandooren@imec.be) and Aaron Thean (Aaron.thean@imec.be).

Electrical characterization and modelling of trap-assisted tunneling in IIIV TunnelFETs

As CMOS technology is entering the 10nm and sub-10nm technology era, the semiconductor industry is faced with a number of challenges that will require important innovations in materials, device design and even the device concept itself. As the gate length is scaled down to 10nm, control of the short channel effects will be one of the key challenges.

Steep subthreshold devices are needed with extremely low supply voltage operation to maintain high current and acceptable leakage. Tunnel-FETs are a promising candidate because they can offer subthreshold slopes below the 60mV/dec thermal limit of MOSFETs thanks to their operation based on band-to-band tunneling at a pn junction.

Tunnel-FETs require direct band-gap materials with low effective bandgap at the tunneling junction to ensure large band-to-band tunneling current at power supply voltage down to 0.5 V and below. Their implementation will
therefore likely require III-V hetero-junctions. At imec, both planar and vertical integration of III-V TunnelFETs are developed.

One main limitation of TunnelFETs is related to the presence of trap-assisted tunneling which turns at low electric field and degrades the subthreshold slope of the devices. Trap-assisted tunneling is due to defects present in the devices, either inside the semiconducting material, at the gate dielectric interface or inside the gate dielectric. In this work, the candidate will focus on the electrical characterization of planar and vertical III-V TunnelFETs using advanced tools. He will use high temperature and cryogenic temperature characterization to extract the different operation mechanisms in the devices, such as band-to-band tunneling, trap-assisted tunneling and Schokley-Read-Hall recombination. He will evaluate the device fabrication method and establish possible correlation with the trap-assisted tunneling component. He will characterize defects present in the devices using various advanced techniques, such as capacitance-voltage, charge pumping or deep level transient spectroscopy (DLTS).

The candidate needs to have an electrical engineering background and strong interest in electronic device physics.

**Type of project:** Thesis project

**Degree:** Master in Engineering majoring in electrotechnics/electrical engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Anne Vandooren (Anne.vandooren@imec.be) and Aaron Thean (Aaron.thean@imec.be).

**Characterization of III-(As,Sb) heterostructures for TFET integration on Si substrates**

In the pursuit of transistor scaling, the tunnel field effect transistor (TFET) is a very promising device for future low-power Complementary-Metal-Oxide-Semiconductor (CMOS) technologies. Furthermore, the large variety of band line-ups and the higher carrier mobilities that III-V materials can offer have made them ideal material systems to make TFET competitive with MOSFETs.

However, the polarity issue between III-V and Si and their large lattice mismatch compared to standard commercially large substrates (like GaAs and Si) are still at the origin of many crystalline defects that can kill device performance. To eliminate these defects, we are studying the influence of molecular beam epitaxy growth conditions on the III-V crystal quality.

The internship, which we are proposing here will hence focus on the characterization of III-V heterostructure materials which are grown on highly mismatched standard substrates (like GaAs and Si). The candidate will be able to work on the large variety of high-tech characterization tools that imec offers. In particular, he (or she) will study the effect of the molecular beam epitaxy growth conditions on the III-(Sb,As) layer quality by means of X-ray diffraction (XRD), Atomic Force Microscopy (AFM), Hall measurements and Transmission Electron Microscopy (TEM). Besides the tool expertise, the learning that the candidate will have during this period is expected to give him a huge knowledge on the defect behavior in these materials and their role on the device performance. Since the candidate will be working in a highly international environment, fluency in English is essential.

**Type of project:** Thesis and/or internship project

**Degree:** Master in Science and Master in Engineering majoring in physics, materials engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Salim El Kazzi (Salim.Elkazzi@imec.be) and Clément Merckling (Clement.Merckling@imec.be).
Transient effects in very high permittivity dielectrics for DRAM applications

Future dynamic random access memories (DRAM) require metal-insulator-metal capacitors (MIMcaps) with equivalent oxide thicknesses (EOT) ≤ 0.4 nm, necessitating the introduction of dielectrics with very high dielectric constant (k~100). Furthermore, low leakage current densities (≤ 1e-7 A/cm²) are required for sufficient retention of charge. Regrettably, high-throughput industrial deposition techniques can result in dielectric films with defects that can facilitate electronic conduction.

The steady-state leakage in MIM structures is now described through trap-assisted conduction mechanisms, while non-uniform electric field due to charge trapped inside the dielectric has to be considered. The general aim of this Thesis will be to theoretically and experimentally study transient effects in the capacitors and separate them into the intrinsic contribution of the dielectric and of the defects. Requirements therefore include understanding of the physics of various conduction mechanisms, trapping and detrapping, and performing electrical measurements and simulations.

Type of project: Thesis or thesis with internship project

Degree: Master in Science and Master in Engineering majoring in physics, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Ben Kaczer (kaczer@imec.be).

Chemical mechanical polishing of new materials

Chemical mechanical polishing (CMP) has become a key step in microelectronic device fabrication: In the deposition step before CMP, an overburden of material is deposited to fill structures with metal material. During CMP, this overburden is removed, removing all metal from the field area while leaving the material inside the trenches untouched (no metal loss). In order to produce faster and more powerful commercial microprocessors, ‘new’ challenging materials such as copper, ruthenium, cobalt, manganese and their alloys need to be polished. For Cu-barrier CMP for example, copper etching should be limited and galvanic corrosion between the copper and barrier materials needs to be minimized. In order to design a CMP process that can achieve this, the chemical reactions that occur between the materials and the CMP slurry need to be understood and controlled.

The scope of this study is to develop a CMP process for the polishing of new materials and to gain a better understanding of the mechanisms that govern this CMP process. The polishing environment is mainly controlled by two factors: the specific materials to be polished and the CMP slurry. The type and combination of materials, the thickness as well as the deposition (e.g. chemical vapor deposition (CVD), physical vapor deposition (PVD), electroless deposition (ELD) or electroplating) and annealing method can be crucial in determining CMP performance. A (metal) CMP slurry uses oxidizers, complexating agents, inhibitors and pH adjusters to achieve a fine balance of chemical reactions that remove material at the surface while keeping corrosion under control by passivating the newly exposed surface during polishing. In this project the effect of various slurry components will be studied both during polishing on our experimental polisher and in a static slurry solution in a lab environment. Surface analysis techniques like X-ray spectroscopy (XPS), X-ray diffraction (XRD) and nano-indentation will provide the necessary extra information to understand which reactions and species are dominant at the surface. The analysis of the data will provide the understanding needed to design a model slurry which polishes the material away at a decent rate while achieving a good quality surface.

If the model slurry design experiments are successful, the efficiency of the optimized slurry will be tested on blanket and/or patterned wafers to make sure that the CMP process removes the required materials with no defectivity or dishing/erosion issues. For this analysis techniques like high resolution profilometry (HRP), defectivity analysis, resistivity and ellipsometry, scanning electron microscopy (SEM) and atomic force microscopy (AFM) can be used.
High quality graphene growth and transfer

Graphene is the name of a two-dimensional, one atom thick material, whereby the carbon atoms are arranged in a chicken wire type ordering. The Nobel Prize Physics was awarded to the 'inventors' of this material, as it exhibits extra-ordinary properties in terms of electrical and thermal conductivity and mechanical strength. Many high technological applications are envisioned ranging from (bio)sensors to interconnects and photonics devices. Initially, the 'synthesis' was done by exfoliating a thin flake from a high tech pencil point, but currently a range of chemical synthesis routes are emerging. These should allow large area, defect free growth of a 2D material. Chemical vapor deposition is the most promising graphene growth technique for technological applications, due to its low cost and possible high quality large area graphene growth. During the graphene synthesis, a carbon containing gas is supplied to a substrate at high temperature. This substrate often contains a transition metal, since these metals possess a high catalytic potential for graphene growth. Nevertheless, the obtained graphene roughness, grain boundaries and control over the number of graphene layers are still a bottleneck for the implementation of CVD graphene in semiconductor applications. Some of the issues could be solved if graphene is grown epitaxial on top of a crystalline transition metal surface. Given the growth temperature and a necessity of a catalytic growth template, a direct graphene growth on electronic devices is unfeasible. Therefore, the development of a scalable transfer method is a second requirement to use graphene in electronic devices. Several transfer process possibility are documented in literature, but up to now, the graphene transfer suffers from contamination often coming from the temporary support layer and/or etching products, wrinkle formation during bonding, crack formation during graphene handling... Resolving the above issues is a must for graphene applications in emerging fields, as currently many 'demonstrations' are still done on exfoliated graphene at a lab scale. In order to achieve a successful and scalable transfer of a thin graphene layer to a target wafer, the graphene layers needs to be lifted from the growth substrate, i.e. the adhesion between both layers need to be minimized. Furthermore, the target wafer needs to be functionalized, so that the adhesion is improved and graphene doping is controlled.

To summarize, the first goal is the growth of high quality graphene layer, with a controlled number of layers and a low defect density. The second goal is to develop a reproducible and scalable transfer method, so that graphene can be integrated in electronic devices.

Type of project: Thesis or internship project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Steven Brems (steven.brems@imec.be) and Ken Verguts (ken.verguts@imec.be).
Defect reduction in Directed Self Assembly processes

In recent years, directed self-assembly (DSA) has emerged as a promising and complementary patterning option for continued scaling (pattern density increase) in the coming years, while maintaining relative low processing cost. DSA processes use block co-polymers to pattern uniform line-space patterns or arrays of holes with resolutions much smaller than the capabilities of the current lithographic exposure systems. For this purpose DSA is actively pursued by various research/industrial groups around the globe. Several figures of merit have been identified and put forward as major checkpoints to assess the relevance of DSA processes for high-volume manufacturing environment; defectivity, roughness, placement accuracy, repeatability and robustness, cost of development and implementation being some of the important ones.

Your project will focus on one of the main factors that would make or break the show for DSA to be adopted by the IC manufacturers/production fabs – reducing the number of defects on the wafer after DSA and to be able to identify their root causes. Defects can be induced by various factors: non-ideal assembly (external and/or on-wafer) conditions, DSA material(s)-induced defects, non-DSA processes related defects (e.g. etch processes) and additionally in most cases, a cross-interaction of the above factors. One of the challenges in this study is to be able to identify/isolate the impact of the above factors on the different defect types we see after DSA. A routine part of this project will involve getting accustomed to advanced lithography tools (in our 300 mm production line environment), like immersion scanners/track clusters to define our process wafers and metrology tools like optical defect inspection, SEM-based defect review, CDSEM and offline software packages for data analyses.

The main goal of your Masters’ thesis/internship is to support and enable the defect reduction strategies of the DSA program at imec in the line-space and/or the contact hole DSA patterns. For this, you will leverage on the 14 nm half-pitch chemo-epitaxy DSA flow for line-space patterns developed in-house and on all the know-how about defect inspection/review strategies, both internally at imec and from external partners. A major part of your tasks will include running the weekly defectivity monitor flow and analyzing the data from it, which acts as the baseline to assess the impact of the various defect reduction approaches we adopt.

Generic DSA literature:

Project specific literature:

Type of project: Thesis and/or internship project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Roel Gronheid (gronheid@imec.be) and Hari Pathangi (pathangi@imec.be).
Exploring novel device applications of III/V materials on patterned Silicon

The monolithic integration of III/V on silicon substrate has gained huge interest due to the potential applications of electronic and optoelectronic III/V devices on Si-based integrated circuits (ICs). This research field is also extensively investigated due to the current CMOS scaling approach beyond the technology node N14. Beside new device designs and architectures such as FinFet and Gate-all-around (GAA)Fets, new channel materials are explored to improve the next generation device performance.

Very promising candidates to replace the Si-channel are Germanium and III/V compound materials due to their high carrier mobility. In addition the direct band structure and hence effective photon emission of most III/V materials allow for the integration of optoelectronic devices such as laser diodes, detectors and modulators on ICs. Nevertheless, the defect-free monolithic integration of these novel materials is a huge challenge due to their large lattice mismatch with Si. The lattice constant of most III/V materials of interest e.g. InGaAs is larger than the one of Si. Therefore the epitaxial deposition of these materials does immediately initiate the formation of misfit and threading dislocations to compensate the lattice mismatch.

It is of key importance to control and reduce the defect density in the active device region to guarantee good device performance. Currently, different integration approaches are investigated to control the defect formation. One of them is the growth of III/V materials between shallow trench isolations (STI) with high aspect ratio. Nucleated defects such as threading dislocations are trapped by the STI side walls deep in the trench to achieve a top III/V layer with low defect density (aspect ratio trapping (ART)).

The topic of this thesis is to explore possible device applications of III/V compound materials integrated on Si substrate:

- Structural and optical characterization of different III/V compound materials such as GaAs, InGaAs, InAs and GaSb grown by MOVPE (metalorganic vapor phase epitaxy) on STI patterned wafers.
- Systematic and comparable study of the defect formation in these various III/V material systems in different trench widths.
- Understanding of the fundamental growth behavior in different trenches as a function of applied MOVPE conditions and chosen precursors and their impact on crystal quality.
- This will lead to the exploration of possible device applications in the field of optical I/O and CMOS.

The student will get an insight into MOVPE and be introduced to different characterization techniques such as X-ray diffraction (XRD), scanning electron microscopy and photoluminescence measurement. Additional techniques will be considered depending on the need. In the frame of this thesis, a basic understanding of different device architectures needs to be developed in order to evaluate application possibilities. Experimental work is carried out in the 300mm production clean room as well as in other labs at imec. This master thesis could possibly be extended to a PhD topic.

Type of work: 20% literature, 40% experimental work, 40% analyzing, simulating and understanding

Type of project: Thesis and/or internship project

Degree: Master in Science and Master in Engineering majoring in physics, materials engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Bernardette Kunert (Bernardette.Kunert@imec.be), Yves Mols (Yves.Mols@imec.be) and Weiming Guo (Weiming.Guo@imec.be).
Visualization and inspection of crystalline defects in high mobility semiconductor materials

In order to continue CMOS scaling for the 7 nm node and below, the integration of advanced semiconductor materials such as Germanium (Ge) and III-V compound semiconductors (InGaAs, InAlAs) is indispensable. This is mainly due to the fact that the charge carriers inside the latter materials exhibit significantly lower effective masses and hence offer enhanced mobility and injection velocity values in comparison with silicon (Si). This in turn facilitates the fabrication of transistors with increased switching speed. Although Ge and III-V compound materials can be grown epitaxially on Si substrates to date, the large differences in lattice constant and material characteristics typically lead to very high defect densities in these layers, causing a degradation of the material properties (i.e. carrier mobility) and hence device performance. For this reason, a qualitative and quantitative assessment of the defectivity of such layers is of utmost importance. While transmission electron microscopy (TEM) can be used to quantitatively determine the defect density in structures containing many defects, the technique fails in case of lower defect densities due to the small sampling volume and the limited field of view, respectively. Chemical etching, on the other hand, can be used to decorate (i.e. visualize) crystalline defects as etch pits or grooves on the layer surface and therefore allows inspection and counting of these etch features at lower magnification, i.e. larger field of view. The purpose of this project is to extend existing etching recipes and apply the latter to decorate defects in nanometer scale SiGe, Ge and III-V structures. In order to visualize and count the generated etch features, appropriate procedures and algorithms using in-line full wafer mapping tools, e.g. based on electron microscopy and/or optical bright-field inspection, need to be developed. It also has been shown that crystalline defects often lead to morphological finger prints on the layer surface (i.e. surface imperfections) of as-grown epitaxial structures. In the second phase of this study the student will therefore explore how bright-field inspection tools can be used to detect those surface imperfections and how their density correlates with the actual defect density determined by defect etching. The experimental part of the work will be carried out in imec’s state of the art 300 mm cleanroom.

Type of work: 10% literature study, 60% experimental work, 30% analyzing and understanding

Type of project: Thesis and/or internship project

Degree: Master in Industrial Science and Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Andreas Schulze (Andreas.Schulze@imec.be).

Optical characterization of 2D transition-metal dichalcogenide semiconductors

Recently, there is a growing interest in the family of two-dimensional (2D) transition-metal dichalcogenide semiconductors MX2 (M stands for Mo or W and X stands for S, Se or Te). The most extensively studied member of this family is MoS2. The latter is an indirect bandgap material in its bulk form, however, becomes a direct bandgap semiconductor (Eg=1.88eV) when thinned to a monolayer. Such a wide bandgap and the structural similarity with graphene makes the material an interesting candidate for potential applications in logic electronics. The most common fabrication procedure for single to few-layer MX2 is mechanical exfoliation (“scotch tape method”) from high-quality natural bulk MX2 crystals. However, exfoliation techniques suffer from small flake sizes and yield limitations which prevents the technique from being adopted for large scale applications. For this reason, imec is currently exploring various methods for growing high-quality large-area few-layer MX2. In order to support the development of such processes, adequate metrology capable of analyzing e.g. the layer thickness, the crystalline orientation and the layer stacking need to be provided, too. This becomes particularly challenging due to the limited volume available for probing as well as the demand for non-destructive techniques with mapping capabilities.
Recently, optical second harmonic microscopy has shown great potential in characterizing mono- to trilayer MoS2 with respect to crystal orientation, domain size and layer stacking. This is possible since few-layer MoS2 (for odd numbers of layers) lacks inversion symmetry and hence allows strong second harmonic generation (SHG). Such a nonlinear optical effect can thus be used for fast and noninvasive characterization and can furthermore be applied to any substrate with weak second-order nonlinearity. Moreover, SHG could be a useful tool for monitoring material modifications which may occur during device fabrication, e.g. patterning or gate stack deposition.

The goal of this internship is to explore and understand the possibilities of optical second harmonic microscopy to study the nonlinear optical properties of MoS2 and to correlate the latter with layer properties such as thickness, orientation, layer stacking and process induced modifications. The measurements will be correlated with more established techniques such as photoluminescence and Raman spectroscopy.

Type of work: 20% literature study, 40% experimental work, 40% analyzing, modeling and understanding

Type of project: Thesis and/or internship project

Degree: Master in Science and Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s): For further information or for application, please contact Andreas Schulze (Andreas.Schulze@imec.be).

Optical characterization of high mobility materials for next generation transistors

In order to continue CMOS scaling for the 7 nm node and below, the integration of advanced semiconductor materials such as Germanium (Ge) and III-V compound semiconductors (InGaAs, InAlAs) is indispensable. This is mainly due to the fact that the charge carriers inside the latter materials exhibit significantly lower effective masses and hence offer enhanced mobility and injection velocity values compared to silicon (Si). To date, Ge and III-V compound materials can be grown epitaxially on Si substrates, however, the large differences in lattice constant and material characteristics typically lead to very high defect densities in these layers, causing a degradation of the material properties (i.e. carrier mobility) and hence device performance. As a consequence, assessing the crystalline quality of these layers is of utmost importance. For this purpose, optical techniques such as photoluminescence (PL) are particularly interesting due to their non-destructive nature and robustness. In PL, excess carriers are generated by laser illumination while the luminescence as a function of photon energy or wavelength is recorded. Crystalline defects typically lead to additional (non-radiative) recombination channels modifying the luminescence spectrum compared to the one of a perfect crystal. In case of nanometer size 3D device structures (e.g. nanowires), however, excitons can also recombine at the surface of the structure. Under such circumstances one measures surface/interface properties rather than the actual bulk crystal quality. In this project the student will therefore assess whether a proper surface passivation of Ge and III-V structures can effectively reduce the surface recombination. For this purpose, the efficiency of different surface treatments and their impact on the luminescence spectrum shall be explored. In the second part, the possibility of time-resolved PL for assessing the material quality will be investigated. To do so, the student will analyze whether the bulk recombination can be distinguished from the surface contribution by fitting the decay of the luminescence signal over time, thereby isolating the various recombination mechanisms. In order to facilitate the study, dedicated test samples need to be developed and cross comparison with other defect characterization techniques (e.g. electron microscopy, defect decoration...) will be carried out.

Type of work: 20% literature study, 40% experimental work, 40% analyzing, modeling and understanding
Surface functionalization routes to enable template-assisted metal nano-interconnects

As the total transistors and interconnects sizes come down to few tens of nanometers and below, a shift in paradigm for the manufacture and integration of microelectronics components becomes apparent. Organic molecules - owing to their size, mechanical flexibility and chemical tunability - fit well in this slot and, thus, are expected to play a key role in IC downscaling. In this respect, self-assembled monolayers (SAMs) seem the best candidates. SAMs are a prototypical form of nanotechnology: the SAM precursor molecules carry the “instructions” required to generate an ordered, nanostructured material without external intervention. SAMs demonstrate that molecular-scale design, synthesis, and organization can generate macroscopic materials properties and functions. Although the details of the thermodynamics, kinetics, and mechanisms of assembly will differ significantly, these monomolecular films establish a model for developing general strategies to fabricate nanostructured materials from individual nanometer-scale components. Because SAMs can assemble onto surfaces of any geometry or size, they provide a general and highly flexible method to tailor the interfaces between nanometer-scale structures and their environment with molecular (i.e., subnanometer scale) precision. SAMs can control the wettability and electrostatic nature of the interfaces of individual nanostructures and thus their ability to organize into large assemblies adding chemical functionality, thermodynamic stability (e.g., improving the adhesion at the dielectric/metal interface).

In particular, metallization of SAMs, i.e. the formation of metallic overlayers or metal clusters on top of monomolecular organic films, is of great importance for many areas of fundamental and applied research, such as metal interconnects. Albeit this topic was actively explored in the last years, reliable methods to the deposition of metal on top of the SAM are continuing to be a topic of intense research. Both selective wet metal deposition techniques and vapor phase metal deposition techniques will be investigated in this study with the final purpose of achieving template-directed metal nanowires with sub-10 nm critical dimensions.

Effect of pH on removal of plasma-deposited fluorocarbon polymer and metal corrosion

In back-end of line (BEOL) processing of advanced microelectronic CMOS integrated circuits, conductor lines are made in a damascene approach by locally etching dielectric layers using plasmas through a patterned photoresist/metal hardmask layer and filling the transferred patterns with copper. During the etching of porous dielectrics using fluorocarbon-containing plasmas such as CF\textsubscript{4}, CH\textsubscript{2}F\textsubscript{2}, and C\textsubscript{4}F\textsubscript{8}, fluorocarbon polymers are formed and deposited on the created dielectric sidewalls. These polymers (≈ “post-etch polymer residues”) are needed to ensure etching anisotropy, profile control and to minimize dielectric degradation. However, they must be removed
afterwards to achieve high adhesion and good coverage of the material (metal) deposited in later process steps in the etched features. Removal of these polymers is challenging, and usually performed by a combination of a short plasma treatment and wet clean using chemical solutions, or by wet cleans alone.

The goal of this project is to study the effect of chemical solutions of different pH on the

- Removal (dissolution and/or lift-off) of fluorocarbon polymer deposited during etching of porous dielectric films.
- Corrosion of the metals and liner materials present in BEOL stacks. The effect of inhibitors on metal corrosion will also be investigated.
- Possible change in properties of SiOCH dielectric films.

Main characterization techniques include:

- Fourier transform infra-red spectroscopy (FTIR) to determine functional groups and bonding structure (polymers and dielectric films).
- Spectroscopic ellipsometry (SE) and porosimetry to determine thickness, refractive index (polymers and dielectric films), and porosity (dielectrics).
- Contact angle to evaluate surface wettability.
- Four-point probe to measure sheet resistance (metals).
- Atomic force microscopy (AFM) to assess surface roughness and morphology.
- X-ray photoelectron spectroscopy (XPS) to quantify surface composition and bonding structure.
- Capacitance measurement to determine dielectric constant.

**Type of project:** Thesis with internship project

**Degree:** Master in Science and Master in Engineering majoring in chemistry, materials engineering

**Responsible scientist(s):**
For further information or for application, please contact Quoc Toan Le (QuocToan.Le@imec.be) and Els Kesters (Els.Kesters@imec.be).

**Quantum mechanical investigation of band-to-band tunneling transitions in advanced heterostructure TFETs**

As scaling of semiconductor components enters the nanometer regime, the increase in power density becomes an important bottleneck. The root cause lies with the 60 mV/dec limit on the subthreshold swing of a classical MOSFET, which causes large leakage currents if the supply voltage is scaled too aggressively.

Alternative transistor concepts, based on quantum mechanical tunneling, are able to circumvent the subthreshold swing limit thanks to their different current injection mechanism. Among the most promising concepts in this category is the tunnel-FET. The tunnel-FET relies on band-to-band tunneling, which allows for sub-60mV/dec subthreshold swing and low leakage currents. Two major tunneling mechanisms provide the current in a tunnel-FET: direct tunneling and phonon-assisted tunneling. Depending on the material, one or the other will be dominant.

One of the greatest challenges that tunnel-FETs face today is that the on-currents which are reached, are still too low. Research is therefore focusing on III-V-based heterostructures, which exhibit a high tunneling probability and therefore a high on-current. It is, however, unclear whether phonon-assisted tunneling can dominate the performance at particular operating conditions. Up until now, direct tunneling has been assumed to be dominant for all III-V combinations and operating conditions. However, phonon-assisted tunneling is expected to play an important role as well.

In this master thesis, the student will therefore carry out a theoretical investigation on the effects of phonon-assisted tunneling in heterostructure tunnel diodes and tunnel-FETs. The student will have access to an in-house developed quantum mechanical simulator to assess the interplay between the direct and phonon-assisted tunneling currents for various material combinations. The student will have to extend the quantum mechanical simulator to allow a thorough analysis. The results of this analysis will lead to recommendations on material choice and optimization of future heterostructure tunnel-FETs.
For this challenging topic a good knowledge of semiconductor physics and semiconductor devices is required, as well as a solid background in quantum mechanics. The research will be carried out in the tunnel-FET team at imec, which has extensive experience in characterization and quantum mechanical modeling of tunneling-based devices.

**Type of project:** Thesis project

**Degree:** Master in Science and Master in Engineering majoring in physics, electrotechnics/electrical engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Devin Verreck (verreck@imec.be).

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**Atomic layer deposition of single and few layer transition metal dichalcogenides: growth and surface chemistry**

Two-dimensional materials are promising new channel materials of the field-effect transistors (FETs). Their atomic scale thickness is an obvious benefit for ultimately scaled electronic devices. Most likely the best known example of a 2D material is graphene. It has exceptional physical and electrical properties but behaves as a semi-metal for which a band gap is absent. The family of transition metal dichalcogenides (MX2) exhibits versatile properties complementing those of graphene [1], and depending on the type of metal and chalcogen does have an electronic band gap. In a single layer of MX2, the transition metal (e.g. W, Mo) is covalently bonded to the chalcogen atom (e.g. S, Se, Te), whereas individual layers of MX2 are only weakly bounded to each other by Van der Waals forces. Recently, they have been integrated as channel material into field-effect transistors (FETs) using mechanical exfoliation and proven to be promising [2]. Interestingly exfoliated single and few layered forms of MX2 do not only preserve their properties, but quantum confinement effects can also lead to additional characteristics. Unfortunately, exfoliation is a laboratory process which is not scalable to an industrial environment where large areas need to be coated instead. A large-area, full wafer deposition technique that still provides control at the atomic level of structure becomes indispensable.

The growth of these ultra-thin, nanometer scale films is challenging since a highly controlled structure and number of layers is desired across a full wafer area. In this project, we will investigate how to grow single and few layered MX2 by atomic layer deposition (ALD). ALD offers growth precision at the atomic level through self-limiting chemisorption reactions at the substrate surface. Volatile precursors containing the film constituents, flow across the deposition surface sequentially and chemisorb locally at reactive surface sites. The surface reactions become self-limiting by exhausting available surface sites and steric hindrance of the chemisorbed precursor molecules. On the other hand, reactions in the gas phase are avoided by exposing the precursors sequentially. The feasibility of the direct ALD MX2 approach is suggested by limited reports in literature [3], although it is not yet understood how to grow single and few layers of MX2 using ALD.

The primary objective is to understand how to grow single and few layered metal dichalcogenides by ALD on a model substrate (e.g. TiN, Al2O3). All depositions are performed at an industrial deposition platform inside imec’s state-of-the-art cleanroom. Both Rutherford backscattering spectroscopy (RBS) and X-ray photoelectron spectroscopy (XPS) are essential characterization techniques to this topic. The concise amount of film constituents as deposited can be measured and related to film thickness, together with insight in the surface composition and chemistry. MX2 materials are both optical and Raman active. Therefore both photoluminescence and Raman spectroscopy can provide essential information about the number of individual layers deposited. When a controllable deposition is yielded, the physical properties of the film including structure, crystallinity and continuity are investigated. To study the continuity of the grown film, a combination of both time-of-flight secondary ion mass spectrometry (ToF-SIMS) and atomic force microscopy (AFM) delivers concise insight in the growth mode of MX2 films; either island-like growth resulting in non-continuous and rough films, or 2D layered growth resulting in more continuous layers.
The project starts with a literature survey and the majority of the work is experimental. The gathered experimental results serve to construct a growth model of the MX2 ALD reaction sequence and gain insight in physical properties of the deposited films.


**Type of project:** Thesis or internship project

**Degree:** Master in Science majoring in chemistry

**Responsible scientist(s):**
For further information or for application, please contact Annelies Delabie (Annelies.Delabie@imec.be).

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**Carbon nanofoams for EUV pellicle applications**

During conventional lithography, adsorption of particles on the mask can print on the wafer adding unwanted features to the wafer pattern. To eliminate these defects, a pellicle membrane is mounted above the pattern so that any particle that falls on the pattern side of the mask is held above the imaging focal plane, where the patterns are located. The pellicles must be virtually transparent to the incident exposure light, mechanically stable during mounting and use in the scanner, and durable to the exposure radiation and scanner atmosphere. For the relatively mature 193 nm lithography technology, the pellicle is made of a thin fluoropolymer material. For the emerging extreme ultra-violet (EUV) lithography however, these fluoropolymers are too absorptive. Instead, novel material solutions must be developed to withstand the EUV light and scanner environment.

![Figure: Scanning electron micrographs of C nanosheets (left) and interwoven C nanotubes (right).](image)

The aim of this project is to investigate new materials that can be used as pellicles for EUV lithography. The focus will be on the fabrication of porous nanomaterials, such as novel carbon nanofoams. Porous nanomembranes offer a tradeoff between mechanical stability and the density of absorbing atoms. At low densities, fewer atoms interact and thus the EUV light transmission increases. Fabrication options include catalytic CVD of Carbon nanosheets or nanotubes on metallic foams. When such the nanosheets or nanotubes are interconnected (“interwoven”), they can form a continuous thin film. To act as EUV pellicles, these films will have to be processed into free-standing membranes with thicknesses well below 100 nm. Developing thin, low density membranes with good mechanical stability is a challenging research topic.

The thesis will include work on the preparation of thin films of Carbon nanofoams, the patterning into free-standing membranes and the characterization of their properties, in particular their mechanical behavior. The student should have an interest in experimental work of thin film deposition, processing, and characterization.
**Spin wave devices for beyond CMOS applications**

Current semiconductor-based CMOS devices may reach their physical limits in the next decade. To be able to continue the scaling of the device dimensions, to improve the device performance, and to further lower the power per operation, the replacement of CMOS transistors by novel types of devices may become necessary. Currently, a number of such devices are being considered, such as devices based on the interference of spin waves (magnons). To be competitive with conventional CMOS, such magnonic devices need to use spin waves with short wavelengths below 100 nm. This requires their miniaturization down to the nanoscale. In this regime, the spin waves are driven by the exchange interaction instead of the dipole-dipole interaction that is dominating at larger wavelengths. Such exchange spin waves are experimentally challenging since their excitation requires the generation of oscillating magnetic fields on very small length scales, of the order of the spin-wave wavelength. For this reason, conventional excitation structures using microwave waveguides in the micrometer range cannot be used efficiently for the excitation of spin waves in the exchange regime. Therefore, novel miniaturized nanoscopic structures need to be designed, for example based on point contacts. Within this thesis, the student will fabricate such structures by e-beam lithography and contribute to the measurement of their electric properties in the microwave frequency range. These structures will be also very useful to measure the properties of the exchange spin waves, such as their dispersion, their damping and their propagation characteristics in the linear and non-linear regimes. The student should have a strong interest in nanofabrication in a cleanroom environment as well as in leading edge research topics on magnetism and magnetic materials.

**Modeling electron transport in graphene-based interconnects**

Semiconductor industry has so far successfully tried to keep up with Moore’s law, increasing the computation power enormously in the last decades. To achieve this, not only the transistor had to scale down with each technology generation, but the whole chip structure needed to be adapted for performance improvements. In particular, the wires that connect the transistors, also known as interconnects, necessarily had to become smaller and smaller. Currently, the wires have become too small, leading to a dramatic deterioration of their transport properties, a major issue for continuing Moore’s law.
One of the possible solutions for improving the wire performance is to find an alternative material with better scalability. While currently copper wires are used, a promising alternative is a graphene-based interconnect. For a better understanding of this alternative, both experimental and modeling studies are required. This master thesis will focus on modeling the transport properties of a graphene-based interconnect. More specifically, the student will adapt a model developed at imec, describing the transport properties of copper nanowires, to simulate a graphene nanoribbon, in order to obtain conductivity, electron relaxation times, mean free path etc. Understanding of electron transport and scattering theory and writing the simulation code form a large part of the master thesis, therefore prior knowledge of quantum mechanics and basic programming skills are recommended.

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in physics, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Kristof Moors (Kristof.moors@imec.be) and Antonino Contino (Antonino.contino@imec.be).

**Transmission electron microscopy: more than an image**

Transmission electron microscopy (TEM) is an essential analysis technique for the development of advanced 3D semiconductor devices. It allows imaging of device structures with very high spatial resolution in different modes as well as chemical analysis of the local composition with sub-nanometer resolution. Interpretation of the images for metrology purposes is generally directly possible. However more advanced interpretation for extracting detailed (quantitative) materials properties requires further analysis of the images or spectra. E.g. strain analysis at defects and in devices can be done in several ways based on either high resolution lattice images or diffraction patterns, compositional analysis can be based on image contrasts or with X-ray or energy loss spectra, etc. For all these applications several software packages are available. The obtained results will be dependent on selected parameters and procedures in the software and may vary between different packages. The work is focusing on the evaluation of different software packages for advanced interpretation of TEM results and application to different topics (strain, compositional analysis) making use of the vast database of TEM measurements of imec. The goal will be to determine best practices for several use cases and applications. It will require that the student obtains an excellent insight in the basics of electron beam/materials interactions and TEM image formation as well as of the materials properties that are investigated. Interest in materials and crystallography is therefore needed. The work is not focusing on software development or own use of the TEM instruments.

Ref: ImageEval; http://en.wikipedia.org/wiki/Multislice; http://tem-s3.nano.cnr.it/?page_id=2

Type of project: Internship project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Hugo Bender (Hugo.Bender@imec.be).
Seeding and growth of boron-doped diamond thin films

Diamond is outforming other materials in many domains such as hardness, wear resistance, thermal conductivity, chemical inertness, and biocompatibility. As it can be made electrically conductive (p-type) by boron doping, boron-doped diamond thin films look especially attractive for electrical applications. They are being explored and developed for a wide range of applications including chemical treatment (e.g. waste water, swimming pool, chemical solutions), nanoscale electrical probes, implantable bio-electrodes, and water splitting/hydrogen generation.

The goal of this internship is to obtain better insight into the interfacial growth of boron-doped diamond layers. For this, the student will seed and grow diamond layers using imec’s hot-filament chemical vapor deposition (HFCVD) reactor using different doping levels, seeding densities and growth parameters. The electrical analysis at the nanoscale is carried out on the interfacial side using electrical AFM methods such as SSRM and conductive AFM (c-AFM) for studying the grain and grain-boundary conductivity. Here, we look for a correlation between boron doping level and grain conductivity. Furthermore, a comparison of doped versus undoped diamond seed nano-crystals is done. The conversion of a seed layer into a highly conductive interfacial layer is not completely understood yet and is therefore investigated in detail in this study. For physical analysis, scanning electron microscopy (SEM), RAMAN, and elastic recoil detection (ERD) are used.

For this topic, the student will work inside a lab and cleanroom environment to carry out the required experimental steps. The student will characterize the fabricated samples by different characterization techniques. The student will be part of imec’s materials and component analysis group.

Type of project: Internship and/or thesis project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Thomas Hantschel (Thomas.Hantschel@imec.be).

Strain characterization inside advanced nano-electronics device structures by enhanced Raman spectroscopy methods

Strain engineering is used as a concept in most advanced nanoelectronics transistor structures to enhance the mobility of electrons (or holes) in the channel region and thereby increasing the channel conductivity. This is achieved by various approaches (e.g. strain-inducing capping layers, using a silicon-rich solid solution such as SiGe). PMOS and NMOS respond differently to the applied strain. PMOS benefits from applied compressive strain whereas NMOS performance is supported by tensile strain. The use of such stress-engineering implies also the possibility to locally measure the stress inside the channel region. In this topic, the use and optimization of micro-Raman spectroscopy is investigated for measuring the local stress in state-of-the-art finFET transistor structures and other next-generation semiconductor architectures. Raman spectroscopy relies on inelastic scattering of photons where energy is carried away or extracted from the crystal in the form of lattice vibrations. The student will learn to work with a micro-Raman system using different laser wavelengths. The experimental focus is on using the nanometer-scale dimension of the device to locally increase the Raman signal originating from the channel region, as well as the isolation of relevant information from the background using polarization considerations. Given the very complex nature of such local opto-electrical effects, simulations of the problems will be indispensable for the correct physical understanding of the experimental results. Therefore, a strong physics background is required. The student will be trained in working with a Raman system and characterize advanced semiconductor device structures. He/she will be part of the materials and component analysis (MCA) department.
Type of project: Internship and/or thesis project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Thomas Hantschel (Thomas.Hantschel@imec.be) and Thomas Nuytten (Thomas.Nuytten@imec.be).

**Embedded distributed human-machine application for accelerator based metrology**

This work will be executed at imec, which is the leading European micro-electronics research center. Imec does research on a wide variety of front edge micro-electronic devices and applications (transistors, memories, solar cells, ...). To verify the correct fabrication of these extremely challenging new devices (sub-22 nm technology) also high end characterization tools are essential. In this framework accelerator based characterization is recognized as a versatile solution.

This subject involves the development and implementation of distributed embedded object-oriented control application within a Visual C++ based programming environment. In particular, the software will have to communicate with various instruments through Ethernet (TCP/IP) and RS232/RS485 (via Serial-Ethernet gateways) and with the user through a user-friendly graphical interface (GUI) as well as support for a flexible scripting language capability. The goal is to achieve this functionality by developing a high quality software suite, paying attention to inter-process communication, class structures, re-usability aspects, etc.

This project aims at the development of a new software package for the control of an accelerator-based measurement system in a modular way with dialog boxes, menu’s, toolbars, property sheets, etc..

The main tasks will be:

- Analyze the present functional system, and design a completely new high-level class diagram for the envisaged multi-threaded metrology application.
- To implement the necessary communication protocols (with stepper motors, data acquisition, counters) into the Visual C++ environment, with an initial user-interface for testing purposes.
- To design and implement a user-friendly graphical user interface (GUI) and scripting capability to interact with the various embedded modules

The software will be designed such that new devices can be connected and disconnected dynamically during the operation, and should appear as virtual instruments on the screen. The signals from various virtual instruments are accessible to both virtual super-instruments as well as scripts that can be run in a command-like environment. The various instruments should be accessed in parallel, i.e. multiple threads may be needed. Ideally, the software allows access to the control application from various locations (locally and remotely) and by various users (multi-user).

This subject is a challenge for those who wish to specialize themselves in the aspects of programming within a Visual C++ based environment for the development of human-machine interfaces.

Type of project: Thesis or thesis with internship project

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in electrotechnics/electrical engineering, computer science

Responsible scientist(s):
For further information or for application, please contact Johan Meersschaut (Johan.Meersschaut@imec.be).
Ion beam scattering: RBS-channeling on III-V nanowires

This work will be executed at imec (www.imec.be), which is the leading European micro-electronics research center. Imec does research on a wide variety of front edge micro-electronic devices and applications (transistors, memories, solar cells...). The development of the extremely challenging new devices (sub-22 nm technology) goes hand in hand with the development of advanced characterization methods. The present topic is an opportunity to learn about fundamental materials characterization techniques in a state-of-the-art nano-electronics research center. Accelerator based analysis is recognized as a versatile solution for thin film (sub-nm scale) characterizations. At imec, we employ an ion accelerator of max. 2 Mega Volt with two dedicated end stations: one for Rutherford Backscattering spectrometry (RBS), and another for Elastic Recoil Detection (ERD) experiments.

Novel materials processing techniques and characterization approaches have boosted the nanoelectronics industry dramatically. We have witnessed the introduction of high-k materials (e.g. HfO2) replacing the SiO2 insulator in advanced transistors, and metals (e.g. TiN) replacing poly-Si as a gate material. Yet, the introduction of novel materials is expected to be even more substantial in the future. Research is ongoing to replace the semiconducting Si by alternative materials. At imec, we develop processes to grow crystalline (epitaxial) SiGe, Ge, GeSn, GaN, InP and InGaAs nanowires in nanometer-narrow trenches, to be used as novel channel materials in devices with superior electrical performance. The electrical performance of the hybrid structures is critically dependent on the crystalline quality of the epitaxial channel material. Using RBS-Channeling and PIXE-Channeling, one may selectively quantify the crystalline quality of the epitaxial material, even when it is nanostructured in the nanometer-narrow trenches. In this topic, we will investigate the influence of the trench-width on the relaxation of crystalline defects and strain in the epitaxial nanowires.

Description of the work
Using the high-energy ion accelerator at imec, you will acquire RBS-channeling data on epitaxial nanowires grown in trenches with varying width and grown with varying deposition processes. For this, you will establish new optical visualization approaches and ion beam focusing procedures. You will develop algorithms to transform the raw RBS-channeling experimental data into absolute crystal defect concentrations. You will employ your algorithms to correlate the defectivity of the nanostructures with variations in the growth parameters.

Type of project: Thesis or thesis with internship project

Degree: Master in Science and Master in Engineering majoring in physics, materials engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Johan Meersschaut (Johan.Meersschaut@imec.be).

Diamond probes for nanoscale electrical measurements

Diamonds superior properties in terms of hardness, thermal conductivity and chemical inertness make it an excellent engineering material for many applications. It can be made electrically conductive by boron doping. Over the last decade, boron-doped diamond tips have become the ultimate choice for performing electrical measurements on the nanometer scale with high spatial resolution. In contrast to other diamond applications where it faces a strong competition from other materials, doped diamond is really the only material which is able to withstand the extremely high pressures (in the GPa range) needed to establish a good electrical contact on silicon and germanium. The solid diamond tips are made by so-called molding whereby first a pyramidal pit is etched, then it is filled up with diamond and finally the mold is etched away. The pyramidal tip is attached to the end of a metal cantilever beam. Using such probes, state-of-the-art semiconductor device structures can be electrically characterized with nanometer spatial resolution.
The aim of this internship is the development of diamond tips probes with improved spatial resolution and electrical conductivity compared to the existing probes. The probes will be designed, fabricated and evaluated. For this topic, the student will work inside a cleanroom environment to carry out the required microfabrication steps. The student will characterize the prototype probes by different characterization techniques. The student will be part of imec’s materials and component and analysis group.

Type of project: Thesis and/or internship project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Thomas Hantschel (Thomas.Hantschel@imec.be).

Sample preparation influences on SSRM device characterization

Metrology is a key driver in the continuous downscaling of transistors and electronic components as it allows to understand the physical processes inherent to the ever shrinking dimensions. One of those promising techniques for future devices is scanning spreading resistance microscopy (SSRM). SSRM is a technique based on the atomic force microscopy whereby one uses a very fine probe (< 5-10 nm radius) to determine the local variations in resistivity on the cross section of a device by measuring the local spreading resistance (Fig.A).

This technique allows to probe the two-dimensional carrier profile in devices with spatial resolutions as small as 1 nm, which is crucial for understanding future semiconductor devices. The measurements are performed on the cross-section of the sample, implying that making the cross section becomes the first important step: better reproducibility and reduced noise levels can be obtained with improved sample preparation. In view of the future extremely scaled devices in planar and non-planar geometries (TFETS’, Trigate, Finfets...), sample preparation becomes an extremely challenging task, so different solutions have to be taken into consideration and explored.
During the period of the internship:

- you will be trained in the use of the SSRM tool and will be incorporated in the development of the next steps in SSRM metrology.
- you will focus particularly on the effects of different sample preparation techniques on the sensitivity and reproducibility of the SSRM measurements.

Data analysis and interpretation will cover an important part of the work as well: you will apply statistical principles in data collection and will be asked to rule out your results. You will work in an international R&D team where you have the chance to contribute to the next steps in nanoscale metrology.

A good command of English language is required.

Since the research & development is very dynamic, the detailed content of the work will be defined at the moment this project starts.

Type of project: Thesis and/or internship project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s): For further information or for application, please contact Kristof Paredis (Kristof.Paredis@imec.be) and Sabrina Magnani (Sabrina.Magnani@imec.be).

STM resolution improvement by low temperature measurements when applied to III-V materials

For decades, electronics has been dominated by one material (Si) and one architecture (planar MOSFET). However, in order to tackle the new challenges in terms of miniaturization, power consumption and speed, new semiconductor materials such as high mobility III-V (InP, InGaAs, GaSb,...) and architectures (FINFET, nanowire, ...) are being developed. In view of these targets, one must achieve high material quality using the advantages of the 300 mm (soon 450) Si-wafer scale processing. Growth of III-V materials on a Si substrate represents a major challenge due to the lattice mismatch. This inevitably results in a highly defective layer as the strain energy is released through the formation of defects (relaxation). Mobility and electrical properties within these films are then affected by scattering on crystalline defects (dislocations, stacking faults and twins), defects which may act as trapping sites, induce junction leakage and promote the diffusion of elements. An adequate metrology, able to probe the nature of these defects and their impact on the film's electrical properties (charge state, electron density, ...) is then required.

During this work we will take advantages of the Scanning Tunneling Microscopy (STM) technique. STM is well known for its excellent properties in terms of spatial resolution (sub-nm) for topographic analysis and, at the same time, for its capabilities to evaluate electrical properties at very localized areas. This makes STM suitable to investigate at atomistic level crystalline properties and presence of defects. The main objective of this work is to explore and exploit the advantages of performing STM at low temperature (below 90K) where the amplitude of lattice vibration is reduced, improving therefore the quality of the measurements. The initial focus will be on imaging standard/reference samples such as highly oriented pyrolytic graphite (HOPG) at both, room and low temperatures.

Differences due to the temperature will be highlighted and moreover limits of the system will be established. This initial part may also include the possibility to explore properties of different tips (in house mechanically cut vs. commercial ones) and different low-noise amplifiers. The second part of this internship regards the improvement of the spatial resolution, when STM is applied to III-V materials. In this case many other factors play an important role, such as sample preparation, surface oxidation, etc...

A theoretical physical background is essential for the understanding of the measurement data but at the same time, technical skills must be quickly developed to master complex instrumentations.
**Type of project:** Thesis and/or internship project

**Degree:** Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Kristof Paredis (Kristof.Paredis@imec.be) and Thomas Hantschel (Thomas.Hantschel@imec.be).

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**Atomic layer deposition of strontium ruthenate as electrode in metal-insulator-metal capacitors for the sub-20 nm DRAM technology node**

A sub-20nm dynamic random access memory (DRAM) technology node requires smaller size capacitors metal-insulator-metal capacitors (MIMCAPs). Downsizing the physical dimensions for a cell capacitance of 20fF/cell will require materials with a dielectric constant (k) of at least 60. This can be achieved with a 8.5 nm strontium titanate dielectric for an equivalent oxide thickness (EOT) of 0.40 nm a leakage current density of ~10^-7 A/cm² at ±1V [1]. Currently, the main challenge in DRAM for the sub-20 nm half pitch is to lower the dielectric physical thickness below 7 nm while maintaining the same EOT and leakage current density as indicated above. At such low physical thickness, lower-k interface layers will negatively impact the electrical properties. An improved, less defective metal/dielectric interface, can potentially be realized with a lattice matched strontium ruthenate/strontium titanate/strontium ruthenate capacitor stack [2]. Strontium ruthenate (SrRuO₃) is a conductive oxide with a bulk resistivity of ~250 μΩcm [3], which can be used as both top and bottom electrode in MIMCAP. Few reports on atomic layer deposition are available [4,5], but to the best of our knowledge a stack having strontium ruthenate both as top and bottom electrode was not yet realized by atomic layer deposition. Control of the Sr/Ru ratio and oxygen content and the absence of segregated phases (e.g.RuO₂ and/or SrO) will be the main challenges in achieving a well-crystallized strontium ruthenate film. Strontium ruthenate thin films growth and crystallization will be investigated by various physical characterization methods and finally the stack capacitors performance will be evaluated by electrical measurements.


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**Type of project:** Internship project

**Degree:** Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Mihaela Popovici (Mihaela.Ioana.Popovici@imec.be).
**Topological insulators for STTRAM: magnetization dynamics modelling & simulation**

During the past years, there has been a constant demand for electronic devices to get smaller, faster and less power-hungry. Scaling down in nanometer scale, has pushed CMOS technology to its limits and now, instead of classical or semi-classical formalism, a complete quantum-mechanical description is required in order to understand how nano-devices work. It is clear therefore, that in order to scale down more and add complex functionalities to our devices, a beyond CMOS approach is needed. The need for new materials that surpass current silicon technology limitations is evident. Topological insulators (TIs) prove to be such a class of materials: they have an outstanding property of being insulating in the bulk, while they show conducting surface/edge modes. Furthermore, these modes are spin polarized: the momentum and spin are locked, meaning that in each mode, depending on the direction of momentum, the spin orientation will also be uniquely defined and vice versa. Such a property makes the topological insulator an excellent candidate for future spintronic devices.

One of the key goals in spintronic devices is to change the magnetization state, which is now used to encode the information bits, with the use of electric currents. This electric current will be used to exert Spin-Transfer-Torque (STT) on the magnetization vector and ultimately reorient it along a preferred direction. This is basically the concept of STT-MRAM. Modelling such devices and examining their operation is the first step towards designing innovating and power-efficient devices for the future. TIs show properties (large Spin-Hall angle) that make them outstanding candidates for such memory devices.

In this master thesis, the student will gain an in-depth knowledge of topological insulators and will examine the dynamical and steady-state behavior of STT memory devices based on topological insulators. The student will benefit from an in-group knowledge of topological insulators as already some work has been done in this field.

Students who are interested in physics modelling and in this topic, should contact the daily advisor and/or the professor regarding any additional information on the topic. The candidate should have an adequate knowledge of quantum mechanics and magnetism.

**Type of project:** Thesis project

**Degree:** Master in Science and Master in Engineering majoring in physics, electrotechnics/electrical engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Dimitrios Andrikopoulos (dimitrios.andrikopoulos@imec.be) and Bart Sorée (bart.soree@imec.be).

**Modelling of superlattice based nanowire transistors**

As the end for MOSFET-based transistor structures is near, much research worldwide is dedicated to possible alternatives. Modeling tools for these future transistor candidates are scarce — if they exist at all, especially when quantum effects start to play an important role. With this in mind, this thesis will contribute to the understanding of superlattice-containing nanowires by using and elaborating upon models and code developed at imec.

The idea behind the superlattice is to form minibands and —bandgaps in the energy spectrum of the wire — much like periodicity of the crystal gives rise to bands in the first place. Electrons entering the device with energies corresponding to these minibandgaps are blocked, which in the end should result in a lower off-current when the transistor is in subthreshold mode, i.e. less static power consumption.

The student will first become familiar with these ideas and the necessary physics to understand the models used, which make use of a simple effective mass approximation. He/she will then elaborate on these models to obtain a more realistic band structure, including anisotropic effective masses, multiple valleys and non-parabolic band bending. The k dot p method could be used to this end. Depending on time and interests, also the effects of exchange correlation or surface charges can be included. In the end, all this can be related again to the formation of the above-mentioned minibands and the resulting current-voltage characteristics for the device.
The candidate should have an interest in quantum mechanics, device physics and some basic notions of programming.

Type of project: Thesis project

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, nanoscience/nanotechnology

Responsible scientist(s): For further information or for application, please contact Maarten Thewissen (Maarten.Thewissen@imec.be).

Novel selector devices for high density resistive switching memory (selector-RRAM)

Resistive Random-Access-Memory (RRAM), based on resistance switching mechanisms, is emerging as a potential nonvolatile memory candidate for below-20nm technology nodes, due to its better scalability, beyond the limits currently predicted for NAND Flash. 10nm-small RRAM cells are shown to have low voltage operation, very fast switching time, in the order of ns and below, small energy consumption per switching and good reliability [1]. To take on the benefits of these excellent attributes to circuit level and enable high density memory arrays implementation, a select device [2] able to enable addressing individual memory cells in an array, without disturbing the others is required. This select device must be scalable, have high rectification ability, following the operation mode of the memory cell (typically bipolar) and enable for high drive current densities, required to switch the memory element.

The main task of this internship/thesis is to screen new materials for selector applications [3,4], get insight into their behavior and assess their viability for selector devices. The work involves development of such devices using a lab-scale process, electrical characterization and analysis of the data. Modeling the observed electrical behavior or physical material characterization may complement this activity, depending on applicant’s background.

You will be using lab-scale processing facilities at imec. You will be using state-of-the-art instrumentation for electrical characterization, you will assist definition of physical characterization experiments and/or use modeling software environments. You will process data and assist in their interpretation.

You must have a good background in materials science or semiconductor physics and general knowledge of the CMOS technology. You are a fast-learner, willing to be trained for lab-scale fabrication process and able afterwards to execute tasks with a high degree of autonomy. You are familiar with data analysis software environments and/or basic instrumentation for electrical testing. You will work in an international R&D team; a good command of English language is required.

The detailed content of the work will be defined at the moment of starting this project, in line with latest research priorities.


Type of project: Thesis or thesis with internship project (duration 6 to 9 months)

Degree: Master in Science and Master in Engineering majoring in electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s): For further information or for application, please contact Bogdan Govoreanu (Bogdan.Govoreanu@imec.be).
Investigation of advanced self-rectifying resistive switching memory Cells (SRC-RRAM)

Resistive Random-Access-Memory (RRAM), based on resistance switching mechanisms, is emerging as a potential nonvolatile memory candidate for below-20nm technology nodes, due to its better scalability, beyond the limits currently predicted for NAND Flash. 10nm-small RRAM cells are shown to have low voltage operation, very fast switching time, in the order of ns and below, small energy consumption per switching and good reliability. To take on the benefits of these excellent attributes to circuit level and enable high density memory array implementation, additional self-rectifying functionality is required for the resistive switching stack [1] and needs to be achieved within a two-terminal, scalable structure.

The main task of this internship/thesis is to investigate new self-rectifying resistive switching memory concepts [2] with the aim of understanding the switching behavior, relate it to intrinsic performance and identify paths for further improvement/optimization and of assessing their potential for dense memory array applications. You will be involved in electrical characterization, focusing on performance and/or reliability aspects. You will be using state-of-the-art instrumentation and you will apply statistical principles in data collection using in-house developed characterization methodologies, so as to ensure a short response time in characterization. You will process data and assist in their interpretation. Feedback for process improvement is a key point.

You must have a good background in semiconductor physics and general knowledge of the CMOS technology. You must be fluent in at least one programming/data analysis environment such as Matlab or similar and familiar with LabView and basic instrumentation for electrical testing. You will work in an international R&D team; a good command of English language is required.

The detailed content of the work will be defined at the moment of starting this project, in line with latest research priorities.


Type of project: Thesis or thesis with internship project (duration 6 to 9 months)

Degree: Master in Science and Master in Engineering majoring in electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s): For further information or for application, please contact Bogdan Govoreanu (Bogdan.Govoreanu@imec.be).

Cleaning of high aspect ratio nanostructures

With the continuous downscaling to smaller feature sizes of microelectronic devices, the semiconductor industry has entered the nano-age. The fundamental limitations encountered with silicon in planar devices has motivated the introduction of new materials, and more importantly, new 3-dimensional architectures. One of the most important process steps is the removal of residues generated by patterning processes. Typically, aqueous based chemistries are used since they have a lower environmental impact and cost of ownership. However, their high surface tension is the cause of unacceptable defectivity from incomplete wetting and pattern collapse.

The contact angle that a liquid drop makes with an ideally flat surface depends mainly on surface chemistry. Amplification of hydrophobicity by surface patterns is frequently seen in nature (e.g. so-called lotus effect). Development of superhydrophobic behavior can lead to processing defects from incomplete wetting in between nanostructures. On the other hand, as the critical dimensions of structures scale down, capillary force can cause significant deflection of high aspect ratio structures and pattern collapse can occur after complete drying. These pattern collapses should be prevented in industrial fabrications. Unexpectedly, incomplete wetting has been observed with nanostructures that have a hydrophilic surface finish.

In this project we investigate the wetting behavior of solutions on nanostructures with different surface chemistries and the parametric dependence of pattern collapse on the wetting properties of the structure material as well as structure dimensions. Our research has evolved to include the evaluation of new characterization techniques to determine wetting depths, the study of wetting and pattern collapse by molecular dynamic simulation (MDS, here basic simulation and data processing skills are required), the study of the kinetics of chemical reactions in nano-confined spaces, and the evaluation of potential solutions for manufacturing. The student will have access to imec’s state-of-the-art cleanroom facilities and get hands on experience of various techniques.

**Type of project:** Thesis and/or internship project

**Degree:** Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Guy Vereecke (guy.vereecke@imec.be) and XiuMei Xu (xiumei.xu@imec.be).

**Gate stack development for high-mobility SiGe channel devices**

As the device scaling is reaching the physical limitation, conventional Si channel is being replaced with high mobility channel materials to keep improving the CMOS device performance. Ge and IIIV channel materials are very attractive candidates according to their bulk properties, however, surface passivation of such channel materials are extremely challenging. Moreover, achieving a sufficient device reliability is a holy grail. SiGe with an increased Ge content is, therefore, the most realistic and the most pressing candidate for the upcoming device generations.
To achieve a high device performance together with sufficient reliability, gate stack structure consisting of metal electrode and gate dielectrics on the channel material, is the key part. Especially, design of the gate stack structure, optimization of the fabrication process, and choice of materials are highly important.
In this project, we are going to do a screening of gate stack materials and processes by using MOS capacitors on 300 mm wafers. The candidate will mainly focus on the electrical characterization, and will evaluate the interface quality, bulk defect density, thermal stability, and scalability of the gate stacks. These electrical characterization will allow us to decide which direction to go for the further gate stack optimization. This project may also include some collaborations with imec’s partner companies to have wide variety of process and material options.

**Type of project:** Thesis project

**Degree:** Master in Engineering majoring in materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Hiroaki Arimura (Hiroaki.Arimura@imec.be) and Aaron Thean (Aaron.thean@imec.be).

**Theoretical investigation of the influence of various scattering mechanisms on the band-to-band tunneling efficiency in III-V tunnel-FETs**

If scaling of supply voltage, and thus power, is to continue novel device concepts are needed. Simple accumulation and depletion mode MOSFETS, however scaled, don't have a steep enough switching behaviour. Because of the thermal distribution of electrons these devices are limited to a switching slope of 60mV per decade of current. One way to achieve sub-60mV/dec switching behaviour is the tunnel-FET (TFET). This is possible because the operating
principle of the TFET is based on band-to-band tunnelling (BTBT). It effectively functions as an energy filter, suppressing the equilibrium thermal distribution of the electrons. However, this theoretical sub-60mV/dec behaviour is not easily achieved in experimental devices. The performance is degraded due to a number of effects caused by, among others, defects and lattice vibrations. Historically, theoretical investigations into the TFET have largely ignored these effects in highly scaled devices, under the assumption that coherent band-to-band tunnelling is the main limiting factor in the electronic transport. Recently, investigation into heterostructure TFET configurations have produced high tunnelling probabilities, which indicate that a coherent quantum mechanical description might be flawed for these structures.

We have developed an in-house solver for the quantum mechanical evolution of a statistical distribution through time. The solver is based on the Wigner-Boltzmann transport formalism, it incorporates both coherent quantum mechanical evolution and decoherence caused by scattering. The candidate should extend this solver to include direct BTBT for III-V devices. With this extension an investigation of the influence of scattering on the BTBT can be performed and the assumption of coherent transport can be verified.

The candidate should have a strong background/interest in solid state physics, quantum and statistical mechanics and computational physics.

**Type of project:** Thesis project

**Degree:** Master in Science and Master in Engineering majoring in physics, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Maarten Van de Put (maarten.vandeput@imec.be).

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**Modelling of spin wave propagation and interference for wave computing**

The main idea behind wave computing is to make a paradigm shift in the way we design devices. Instead of making conventional devices that are part of a logic function, the goal is to make devices that already realize a logic function more functional than just an elementary switch.

Wave computing may realize this and is based on using the information carried by a wave such as amplitude, phase and frequency. The expectation is that one would need less interconnect as this is already part of the device (i.e. the realization of a complex logic function in one device removes the otherwise required local interconnect present in conventional CMOS logic).

Spin wave computing uses magnonic excitations which result in magnetization waves (coined spin waves in literature) propagating in ferromagnetic materials (spin wave bus). In order to excite, manipulate and detect spin waves different possibilities exist: magnetic tunnel junctions, microwave antenna or magnetoelectric elements. Spin wave computation uses interference and phase manipulation to obtain the desired computational outcome.

In this master thesis the student will investigate several spin wave interference devices and/or waveguide structures that may be useful as elementary subcomponents for wave computing devices. For this, the student can rely on a micromagnetic solver or simulation program in order to study the dynamics of the magnetization in such structures. A solid background or interest in magnetism and solid-state physics is required.

**Type of project:** Thesis project

**Degree:** Master in Science and Master in Engineering majoring in physics, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Odysseas Zografos (Odysseas.Zografos@imec.be) and Bart Sorée (bart.soree@imec.be).
Light-matter interaction in organic and inorganic materials for EUV lithography

Extreme ultraviolet lithography (EUVL) is the candidate to scaling down of semiconductor devices beyond the 1x nm technology node.

To realize the required targets in this lithographic technology EUV photoresist play a significant role and more intimate light-matter interaction studies (i.e. absorption and electron yield) are needed to get more fundamental understanding in their mechanism of interaction.

In this frame, the student will have to work with different international research facilities.

The student would have to work at imec to develop the procedure for the sample preparation (i.e. design the sample holder needed for the analyses) and would conduct the experiments aiming to explore various materials by using:

1. Spectroscopic ellipsometer in the wave-length range of 150-750nm
2. X-ray photo absorption spectroscopy (XAS) in the energy range between 5eV and 250eV at the BEAR beamline @ Elettra synchrotron research facility (http://www.elettra.trieste.it/elettra-beamlines/bear.html).
3. Literature studies to understand the physics involved at higher energy ranges (up to 1.5keV)

This work will significantly contribute to the understanding of how different materials interact with the light and will lead to help the design of new photoresists for EUV lithography.

To accomplish his task, the student has to have fundamental understandings of x-ray physics and light-matter interaction. Experience with Matlab software tool is of advantage.

Imec 300mm cleanroom and ASML NXE:3100 EUV tool     BEAR beamline at Elettra synchrotron facility

Type of project: Thesis with internship project

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering

Responsible scientist(s):
For further information or for application, please contact Danilo De Simone (danilo.desimone@imec.be) and Geert Vandenberghe (geert.vandenberghe@imec.be).
True-3D circuit integration

The continued CMOS scaling towards the 10nm, 7nm and 5nm nodes is proving to be more difficult (and thus more expensive) every generation. Still, the need for higher density circuits in consumer products is very real. Making matters even more interesting, many of today’s smart systems (SmartPhone, tablets, SmartWatch) require the seamless integration of more functionality on top of CMOS logic: integrated memory, integrated high-voltage I/O (e.g. USB 3.0), various integrated RF frontends for wireless communication. Existing solutions include stacking multiple chips, using Through-Silicon-Vias (TSV) to make electrical connections. While this approach is feasible in many applications, it has some disadvantages:

- The electrical connections between the different chips are quite long (50-100 micron), which may limit the circuit performance.
- The TSV’s consume lots of silicon area (which cannot be used to make transistors)
- The fabrication of the TSV’s requires a significant amount of extra fabrication steps, adding to system cost.

Therefore, a big need exists to truly explore the 3rd dimension and create real 3D-circuits. Obviously, the fabrication of such 3D circuitry is not straightforward. Imec is in the process of patenting a number of solutions to tackle this problem, preventing the discussion of details in this document.

The master thesis student will join an international team of multidisciplinary scientists and engineers dedicated to implement these solutions. The specific content of the master thesis will be defined based on the applicant’s interests, skills and background and team needs. Specific activities may include (non-exclusive list):

- Investigating how such 3D-circuits can be made using specialized computer-simulation models (TCAD)
- Characterize prototype-chips, attempt to explain their performance and suggest improvements.

Type of project: Thesis project

Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Geert Hellings (Hellings@imec.be), Kristin De Meyer (demeyer@imec.be) and Dimitri Linten (linten@imec.be).
**Layout mapping of Spin-Wave Device (SWD) circuits**

In search for the technology that will extend logic circuits and electronics beyond the CMOS technology and the eminent end of semiconductor scaling, many researchers have focused their efforts in using the spin of magnetically ordered materials as the logic information carrier. A spin wave is defined as the propagating oscillation of magnetization in a ferromagnetic material. As in any wave amplitude, phase and frequency can be defined for spin waves and they can be used for logic computation. This computation scheme is drastically different from the classical boolean logic and offers many advantages. SWD circuits have the potential of being ultra-low power but in order to prove that there needs to be a methodology in place of how the devices should be mapped from a simple netlists to physical designs.

In imec, SWD circuits have been a research focus since September 2013 and we have already gained significant insight and expertise. In this Master Thesis the student will have the opportunity to address the problem of technology mapping and explore different layout approaches that have a big impact on the actual SWC circuit design. Also he/she will be able to quantify that impact by using the evaluation framework already in place here at imec.

The student's tasks will include: literature study of SWD circuits; circuit timing simulations based on SWD technology specifications; algorithmic optimization of mapping from netlists to SWD circuits; system-level evaluation of the mapping; benchmarking and comparison with other Beyond-CMOS technologies already studied and state-of-the-art CMOS nodes. The student should preferably:

- Be flexible using different programming and scripting languages
- Be familiar with logic circuits design and EDA toolflows
- Have working understanding of Micromagnetics and Solid State Physics
- Be interested in circuit and system-level design and benchmarking
- Fluent English speaker
- Be a team player

**Type of project:** Thesis project

**Degree:** Master in Science and Master in Engineering majoring in electrotechnics/electrical engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Odysseas Zografos (zogra@imec.be) and Praveen Raghavan (ragha@imec.be).

**Plasmonics: circuit and system-level evaluation for beyond-CMOS applications**

In search for the technology that will extend logic circuits and electronics beyond the CMOS technology and the eminent end of semiconductor scaling, many researchers have focused their efforts in using plasmons as the logic information carrier. Plasmons (more specifically Surface Plasmon Polaritons – SPPs) are quasiparticles that can propagate on the interface of metals. SPPs can be viewed and used as waves in wave computation circuits that follow different principles from the classically designed boolean logic circuits. Plasmonics technology is promising due to their high speed and small/scalable wavelength.

In imec, we are already studying the potential applications of many Beyond-CMOS technologies along with plasmonics. In this Master Thesis the student will have the opportunity to study and evaluate different concepts of plasmonics circuits and compare them with some of the Beyond-CMOS technologies studied in imec.
The student’s tasks will include: literature study; conceptualization, modeling and simulation of plasmonic devices (with Lumerical FDTD); first order system-level estimation of plasmonic circuits; benchmarking and comparison with other Beyond-CMOS technologies already studied and state-of-the-art CMOS nodes. The student should preferably:

- Be flexible using different modeling/simulation tools
- Have working understanding of Photonics and Solid State Physics
- Be interested in circuit and system-level design and benchmarking
- Fluent English speaker
- Be a team player

**Type of project:** Thesis project

**Degree:** Master in Science and Master in Engineering majoring in physics, electrotechnics/electrical engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Odysseas Zografos (zogra@imec.be), Praveen Raghavan (ragha@imec.be) and Bart Sorée (Bart.Soree@imec.be).

**Top down device and layout exploration for advanced CMOS nodes (5nm)**

The key challenge of any technology definition is the gains that can be obtained in power-performance-area and cost. Assessing these metrics is crucial, this masters topic will attempt to assess various layout styles for LNW Fets, along with device level assessment of its performance-power benefits. The approach would be double folded where the device is approached from the TCAD where compact models would be built and circuit level assessment would be done. And also in a top-down fashion where the target of the device is specified from circuit level and the associated requirements/matches need to be made at the device level. To assess the area impact different layout styles would also be assessed to make appropriate area assessment of different cells. The student would need basic understanding of device physics and circuit design.

**Type of project:** Thesis project

**Degree:** Master in Science and Master in Engineering majoring in physics, electrotechnics/electrical engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Praveen Raghavan (ragha@imec.be).

**Optimization of graphene devices**

Graphene, an atomically-thin sheet of carbon atoms arranged in a sp2 honeycomb lattice, has been successfully isolated for the first time only in 2004 (this achievement was awarded the Nobel prize of Physics in 2010). Ever since, new exciting reports are appearing in literature about the peculiar electronic properties of graphene, which mainly arise from the configuration of its energy band structure, combined with the intrinsically low occurrence of defects and the stiffness of its lattice, allowing for the featuring of intriguing 2-D physical phenomena. Graphene has been proposed as a candidate for many purposes, from electrodes to CMOS and post-CMOS electronics. However, in order to make electronic applications of graphene realistic, one has to necessarily tune its electronic properties, so that, for example, a bandgap can be introduced. Another important aspect of the current graphene research entails the finding of a synthetic alternative to micromechanical exfoliation for graphene production, in order to achieve high quality, large scale graphene, addressable for CMOS-compatible device fabrication.
The objective of this study is to explore new device architectures by manipulating the graphene properties targeting the specs of future technology nodes. The student will learn to handle graphene sheets, fabricate graphene FETs, and characterize their performance. Some of the challenges involved:

- the study of the interaction between graphene and the different active layers in the device (e.g. graphene-metal contacts, gate stack,...); by investigation of the electronic modifications of the graphene properties influenced by its environment
- post-processing of graphene (e.g., transfer, device design and fabrication)
- electrical and/or structural characterization of (integrated) graphene devices

**Type of project**: Thesis and/or internship project

**Degree**: Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, bioengineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

**Responsible scientist(s)**:
For further information or for application, please contact Inge Asselberghs (inge.asselberghs@imec.be) and Dennis Lin (dennis.lin@imec.be).

**Voltage control of magnetic anisotropy**

Control of a magnetic bit by means of an electric field would allow operation of magnetic memories (MRAM) at much lower power levels than the present Spin-Transfer Torque MRAM (STT MRAM). The recently discovered Voltage Controlled Magnetic Anisotropy effect (VCMA) offers perspectives for such voltage control of magnetic bits and will be investigated in this project. Depending on the student's preference either experiments or modelling work can be done or a combination of both.

When an electric field is applied normal to the interface of a dielectric – mostly MgO – and a ferromagnet the interfacial anisotropy of the thin film ferromagnet can be affected. This effect can give rise to the switching the anisotropy of such a thin film ferromagnet between an in-plane and out-of-plane magnetic anisotropy. At present the origin of the effect is discussed in literature and various mechanisms have been proposed to explain the observed effect. In this project the VCMA effect can be investigated experimentally. Alternatively simulation work can be done to investigate how a voltage controlled magnetic memory device can be built.

**Type of work**: 10% literature, 90% experimental work and device fabrication and/or modeling


*Large voltage-induced magnetic anisotropy change in a few atomic layers of iron*  

**Type of project**: Thesis or internship project

**Degree**: Master in Science and Master in Engineering majoring in electrotechnics/electrical engineering, physics, material sciences, applied mechanics

**Responsible scientist(s)**:  
For further information or for application, please contact Koen Martens (Koen.Martens@imec.be).
Impact of pulsed RF source in capacitive coupled plasma etching of common materials used in VSLI manufacturing

CMOS scaling requires to move to thinner films, smaller dimensions, higher aspects ratios. New device geometries imposes to etch different materials each selective to the other, with long over-etch times. This is particularly difficult for dielectric etching, which require high ion energies as catalyst for surface reactions leading to volatile product desorption. Typical chambers for dielectric etch use the capacitive coupled plasma (CCP) geometry, driven by RF generators between 2 and 60 MHz, which lead to the formation of a large self-bias between the substrate and the plasma. Recently, RF pulsing has been suggested as a technique to enhance etch selectivity between various materials. RF pulsing consist in alternating plasma OFF and plasma ON states at a frequency between 10 and 1000 Hz, and with duty cycle (ratio of period ON to period OFF) varying between 10% and 90%. The impact of plasma pulsing has been thoroughly described for inductively coupled plasma (ICP), however pulsing for CCPs is a relatively new subject and there is little or no data existing on its impact on material etch rates.

In the proposed Master thesis topic, we will study the impact of plasma pulsing on the etch rate of various common materials used in VSLI manufacturing. In more details, the impact of changing the pulsation frequency (10 to 1000 Hz), the duty cycle (10 to 100%), will be studied for three RF frequencies (2, 27, 60 MHz) and for various plasma powers (50 to 1500W). The impact of mixed frequencies (2+27MHz, 2+60 MHz) will also be studied. The materials that will be considered are Si3N4, SiO2, OSG low-k, TiN, SiC, PolySi, Photoresist. The etch mechanisms will be studied by means of optical emission spectroscopy (OES) and surface chemical analysis will be obtained by X-ray photoelectron spectroscopy. Materials etch rate and CxFy thicknesses will be measured by means of spectroscopic ellipsometry and mass measurements. A correlation between blanket etch rates tests and patterning results (contact holes, SAC) will be tentatively established.

Type of project: Internship project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact JF de Marneffe (marneffe@imec.be), Ziad El Otell (Elotel89@imec.be) and Mikhail Baklanov (baklanov@imec.be).

Quantification of VUV light emitted during industry-compliant plasma processing and related damage to advanced low-k materials

The drive for high performance and faster electronic devices has led to decreasing the features of integrated circuits (IC) to sub-30 nm dimension. This drive has led to a vast advancement in lithographic techniques and resist materials which made it possible to pattern such dimensions. However, progress in device integration is not possible without an advancement of equal caliber in plasma etching and material selection. Traditional interconnect materials, such as SiO2 having a k-value of 4, were replaced by porous organosilicate (p-OSG) materials, with a k-value of 2.4, which are now becoming a limiting factor as their RC response time is increasing with the shrinking device features. High porosity OSG materials, with k-values as low as 2.2, are being proposed and benchmarked to replace p-OSG with 2.4 k-values. However, these p-OSG materials are highly sensitive to plasma exposure which results typically in an increase of their k-value; especially that these materials will be exposed to different plasma etching/depositing steps in order to achieve the final devices. Plasma-induced damage on low-k materials has been studied extensively during the last decade. Early studies on low p-OSG materials showed that the induced damage is related to radicals, ions and vacuum ultra-violet (VUV) light emitted from the plasma relating it to particular plasma chemistries. Current studies on high p-OSG, ultra-low-k materials, performed in fluorocarbon containing plasmas, show that the induced damage is partly related to VUV emission from the plasma. Almost all materials absorb emissions in the VUV range making optical measurements at such wavelengths extremely challenging. The complexity of the plasma chemistries, lack of literature data on such VUV emission from processing plasma chemistries, the vulnerability of p-OSG to VUV
and the challenging task of measuring the VUV emission pose a serious issue which needs to be addressed to enable the integration of ultra-porous OSG in IC. Within this internship (6 months), it is proposed to address these challenges by enabling the measurement of VUV radiation emitted by these complex chemistries and selectively exposing the p-OSG only to VUV emission and solely assessing its damage. The work will involve getting trained on the use of TEL plasma etch chambers, operation of state-of-the-art VUV spectrometer, characterization of p-OSG by FITR, spectroscopic ellipsometry, ellipsometric porosimetry, water-contact-angle, K-value extraction by the Pt-dot method. In addition, the VUV absorption spectra of various spin-on low-k materials will be tentatively measured by direct transmittance/absorption spectroscopy.

**Type of project:** Internship project of 6 months

**Degree:** Master in Science and Master in Engineering majoring in physics, chemistry, electrotechnics/electrical engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact JF de Marneffe (marneffe@imec.be), Ziad el Otell (Elotel89@imec.be) and Mikhail Baklanov (baklanov@imec.be).
II. GaN Power Electronics

There are currently no Master thesis/internship projects available in this domain.
III. Wearable Health Monitoring

Development of a wearable eye tracker

The Wearable Health Solutions (WHS) group at imec is looking for a Master student to work on an imaging wireless sensor node for eye tracking purposes.

The objective of the project is to make an early prototype of wearable real-time eye tracker based on simple imaging-based sensors and existing off-the-shelf components. The prototype should be used as proof of concept for different applications and to provide data for evaluation and analysis purposes.

The following steps will be followed:

- Literature research on the field of interest (guided by supervisor)
- Imaging study based on readily available tools
- Basic algorithm development based on acquisition of static images
- Study on available embedded platforms for image processing
- Selection of embedded platforms to base functional demonstrator on
- Implementation of algorithms in embedded platform
- Integration of functionality into final demonstrator
- Documentation (report, thesis, etc.)

What we offer:

- Excellent international research working environment
- Insights in the wearable, low power embedded electronics research field
- Valuable skillset for the job market

Desired skills:

- English language (all work will be performed and documented in English)
- Background on Image Processing or Machine Vision
- Software programming (C,C++, Matlab, LabView)
- Experience with microcontrollers (Atmel, Arduino, MSP430, ARM, etc.)
- Knowledge of electronics hardware (making simple schematics, connection of different devices in a system, interfaces in microcontrollers, etc.)
- Interest in biomedical, wearable devices and body area networks
- Independent, self-sufficient worker
- Interested in eye-related aspects

Related fields to the work offered: biomedical engineering, embedded electronics, wearable devices, image processing, video tracking, smart sensors, wireless sensor networks, ultralow power electronics, body area networks, imagers, microcontrollers, sensor design, medical devices, optical measurements, robotics, smart watches, smart clothing, smart glasses, stereovision, tracking.

Type of project: Thesis project

Degree: Master majoring in electrotechnics/electrical engineering, industrial design

Responsible scientist(s): Carlos Agell (carlos.agell@imec-nl.nl)

For further information or for application, please contact Carlos Agell (carlos.agell@imec-nl.nl).
Multi-channel bio-impedance measurement system

Impedance Tomography is non-invasive medical imaging technology based on the electrical measurement data from multiple skin electrodes. Basic concept is the same as single channel bio-impedance measurement, so that AC current is injected into one pair of electrodes, and DC voltage is measured from the other pairs of electrodes. The major difference of Impedance Tomography than single channel bio-impedance measurement is the sweep of electrode combination to have the spatial resolution of the image inside of the 3D geometric model.

The aim of this project is to verify and analyze the advantages of multi-channel bio-impedance measurement over single channel bio-impedance measurement by computer simulation and in-vitro measurement. This project will (partially) consist of the following assignments:

- Literature research on the field of interest (guided by supervisor)
- 3D simulation of multi-channel bio-impedance measurement on simple geometric model
- Prototyping multi-channel bio-impedance based on existing single channel device
- Building a phantom to measure, and performing the measurement
- Basic signal processing algorithm implementation
- Data analysis
- Documentation

In order to perform the assignments successfully, the candidate with the below profile is highly desired:

- Fluent level of English language skill (all work will be performed and documented in English)
- Experienced user of Matlab software
- Knowledge of electronics hardware (building and debugging ability in PCB level is required)
- Experience with COMSOL software is plus
- Interest in biomedical, wearable devices and body area networks
- Independent, self-sufficient worker

Type of project: Thesis with internship project

Degree: Master majoring in bio-engineering, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Seulki Lee (Seulki.Lee@imec-nl.nl) and Victor van Acht (Victor.vanAcht@imec-nl.nl).

EEG headgear optimal designs and process automation

Current electroencephalography (EEG) headgear designs are either developed for covering the complete area where EEG can be measured, which is a typical clinical practice, or they are oversimplified as they include only a few electrodes that cover some parts of the brain (mostly non-hairy one), typically aimed at gaming. Most the existing EEG headgear solutions do not address the end-user needs nor they are designed with for a specific user – use case scenario. The root cause of it is in the diversity of EEG applications, users' preferences, and users' head shapes and sizes.

The aim of the thesis work is to define guidelines for optimal EEG headgear design and specify requirements for automating the process such that it can lead to industrialization. The work will consist of the following assignments:

- Generating overview of existing headgear designs and understanding their deficiencies and benefits
- Understanding end-user requirements for a number of target EEG applications (e.g., epilepsy monitoring, stroke rehabilitation, neurofeedback for peak performance training).
• Detailed exploration of optimal EEG headgear design on a (set of) selected EEG applications. This should include design and development of headgear solutions, as well as feasibility study on industrializing the production.
• Design, development and execution of experiments aimed at evaluating headgear solutions for selected EEG application(s). The outcome should lead to EEG headgear design guidelines.
• Dissemination of result through a demo and a final report or a conference paper.

**Type of project:** Thesis project

**Degree:** Master majoring in electrotechnics/electrical engineering, industrial design

**Responsible scientist(s):**
For further information or for application, please contact Bernard Grundlehner (bernard.grundlehner@imec-nl.nl) and Vojkan Mihajlovic (Vojkan.mihajlovic@imec-nl.nl).

**Intelligent strategies to learn and recognize lifestyle patterns**

Imec has proven track record of wearable technologies for continuous activity and vital signs monitoring. Thanks to the quality and design of our sensor systems and to collaboration with clinical centers and universities we have developed and validated several algorithms for extracting meaningful information on the health status of a subject. We are currently developing “at hand” solutions (such as applications for smartphones and tablets) that can allow users to visualize their health status and receive feedback for improving their condition on routine basis. This master thesis has the objective to contribute to our goal to derive algorithms more and more tailored to the specific user needs.

The aim of the student project is (1) to integrate quantitative vital signs collected by our sensors with qualitative information collected with technologies already available in the consumer market; (2) to develop intelligent algorithms able to learn from the user and capable of recognizing lifestyle patterns; (3) to test the robustness and flexibility of the algorithms with respect to noise and missing data; (4) to contribute to the design of feedback systems able to motivate behavioral changes.

**Tasks:**
- Develop and test innovative multi-parameter algorithms
- Provide technical support for experimental protocols design
- Actively interact with interdisciplinary team
- Write technical reports

**Profile:**
- You have a proven experience with Matlab or Python, and JAVA
- You have a proven experience with machine learning techniques
- You have experience with data collected from wearable devices (preferable)
- You are able to quickly understand problems and discuss analytically solutions within the team
- You like to work independently and are capable to clearly refer to team members and supervisor for technical needs and consultancy
- You have good written and verbal English skills
- You are highly motivated and passionate for wearables, health and data mining
- You are eager to grow in your knowledge and competences

**Type of project:** Thesis project

**Degree:** Master majoring in computer science and engineering

**Responsible scientist(s):**
For further information or for application, please contact Giuseppina Schiavone (giuseppina.schiavone@imec-nl.nl).
Physiologically-derived authentication keys

Securing cloud-based services such as e-mail, data storage, social media, banking and payments rely heavily on passwords. Security systems based on passwords are not user friendly since users have to remember them and they can be weak due to the weak choice of passwords. This growing burden can possibly be replaced by using unique biometric identifiers to unlock such services. New ways to easily measure a multitude of physiological data through smart watches, smart patches and equipment worn around the head can increase the robustness and security of biometric identification.

The aim of the thesis work is to investigate unique personal patterns in each of the available physiological signals that can, either directly or combined with data fusion techniques, lead to extraction of unique and reproducible keys/IDs for the purpose for unlocking cloud-based services.

The work will consist of the following assignments:

- Investigating current state of the art in biometric identification based on each of the physiological signals through a literature study
- Systematically improve state of the art by looking at individual biometric keys and by using data fusion
- Setting up a test bench for validating the proposed mechanism and estimating its performance
- Disseminate the results in a working demo and through final report

Type of project: Thesis project

Degree: Master majoring in electrotechnics/electrical engineering, computer science

Responsible scientist(s):
For further information or for application, please contact Bernard Grundlehner (bernard.grundlehner@imec-nl.nl), Vojkan Mihajlovic (Vojkan.mihajlovic@imec-nl.nl) and Georgios Selimis (Georgios.selimis@imec-nl.nl).

Data visualisation and fusion for Body Area Network sensors

Microsystem technologies are currently stimulating the development and deployment of personal body area networks. These wireless networks provide lifestyle, assisted living, sports or entertainment functions for the user, without visible interference with their active lives. Prevention rather than detection and cure will be the future paradigm.

In imec's imHealthy program, such body area networks (BAN) with several different types of sensors are currently under development: ECG signals, skin conductance, ions in sweat, motion and many more signals can be monitored, recorded and wirelessly transmitted to a hub during longer periods of time.

With the growing availability and acceptance of these sensor networks for improving our life quality, it becomes attractive to use their information in a multitude of applications where the user can directly benefit from this information by managing his lifestyle and health.

Typically these sensors generate a sea of measurement data (especially when capturing data over longer periods of time – i.e. days till months) in which it is a challenge to select the valuable information. However combining information for several sensors can reveal new insights in different domains such as healthy behaviour stimulation, assisted living, stress management, ... Specific challenges are:

- visualize cross platform sensor data (i.e. data from different types of sensors, such as a mix of commercial and research devices) simultaneously over large timeframes
- search for correlations between data of these sensors (e.g. heart beat with skin conductance data for stressed people)
- identify valid sensor data in long time series
- how to summarize the multitude of data in order to give a proper feedback message to the user?
- ...

In this thesis work, first a scan of the state of the art (literature) on sensor data management will be done. Furthermore it is then the aim to elaborate a strategy for a flexible visualisation, markup and analysis (data cleaning
and correlation) tool for heterogeneous sensor data for use on a pc and a mobile device. In a first step available captured data will be used to map sensor data from different sensors and correlate these data from different sensors: heart rate, accelerometer data and skin conductance data will be studied over long time periods (days) searching for strategies to summarize extracted information in a clear and attractive way for the user. Next steps will then increase complexity by fusion of data from a more heterogeneous set of sensors.

**Type of project:** Thesis and/or internship project

**Degree:** Master in Engineering majoring in nanoscience/nanotechnology, electrotechnics/electrical engineering, bioinformatics, bio-electronics

**Responsible scientist(s):**
For further information or for application, please contact Walter De Raedt (Walter.DeRaedt@imec.be).
IV. Life Science

Nano-photonic structures to collect and enhance fluorescence emission on a SiN platform

Silicon photonics has become one of the most promising photonic integration platforms in recent years. The combination of high-index-contrast and compatibility with CMOS processing technology made it possible to use the electronics fabrication facilities to make photonic circuitry. There has been a tremendous interest towards integration of photonic devices in biological sensing and detection recently. The visible and very-near-infrared (500-950 nm) wavelength window is of great interest for this kind of applications due to low photo damage and availability of low-cost sources-detectors. Unlike Silicon (Si), Silicon Nitride (SiN) is transparent in this Visible & Near-Infrared window and provides the combination of high-index-contrast and compatibility with CMOS processing technology. A low-loss silicon nitride platform has been developed here and by an extensive materials study in the 200 nm line of imec, the propagation losses were reduced below 0.5 dB/cm in visible wavelength.

For ultimate integrated fluorescence-based biosensing applications, the development of devices that efficiently both excite and collect fluorescence from dyes located near the chip surface is of paramount importance. In this work, the aim is to investigate the effect of different nano-photonic structures on the fluorescence emission of the dyes residing in the near field of the structures. This investigation will help to develop nano-photonic devices to enhance the fluorescence emission and collect that efficiently by the chip. The student will use FDTD simulation to optimize the design for structures like waveguides, ring resonators and linear resonators. Then (s)he will fabricate them using electron beam lithography. Finally, (s)he will investigate the influence of those structures on the fluorophore placed in the near field. The student will gain hands-on experience with optical experiments. Sample preparation will be handled by the student in the imec III-V cleanroom in cooperation with the daily advisor. The student will obtain experience in optical and electron beam lithography and master various deposition and etching techniques. Further sample characterization will be done by optical microscopy, scanning electron microscopy and waveguide transmission spectroscopy. The candidate should have a strong interest in photonics and nanofabrication.

Type of project: Thesis or thesis with internship project

Degree: Master in Sciences or Master in Engineering majoring in physics, chemistry, materials engineering, bio-engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Md Mahmud-Ul-Hasan (Mahmud70@imec.be).

High performance computing for life sciences

Context
Het lab gebruikt huidige en toekomstige Intel processorzoeken (zoals de allerlaatste Intel Xeon Phi coprocessors), heeft een eigen kleine cluster van 64 compute nodes (meer dan 1200 cores) lokaal, en gebruikt daarnaast de infrastructuur van het VSC (Vlaams Supercomputer Center) voor grotere experimenten.
Binnen het gedeelte van het lab dat de context vormt voor dit voorstel interesseren we ons aan schaalbaarheid (zowel binnen compute nodes als over netwerken van compute nodes), met load balancing (weer zowel binnen als over compute nodes) en het omgaan met hardware fouten.

Doel
Het eigenlijke doel wordt beslist in samenspraak met de student zodat het aansluit bij de interesses van de student binnen de context van het lab. Het zal echter passen in de context van high performance computing voor de Life Sciences. Zie hieronder voor voorbeelden van onderzoeksvragen die kunnen aangepakt worden.

Onderzoeksvragen
Het ExaScience Life Lab is zeer breed, zoals reeds omschreven bij doel. Er is dus ook veel mogelijk. In het algemeen zal het onderzoek te maken hebben met software engineering, parallel programmeren en/of gedistribueerd programmeren. Dit onderzoek zal gebeuren in de context van een concreet probleem dat relevant is voor minstens 1 van de industriële partners (Intel of Janssen Pharmaceutica). Hieronder enkele voorbeelden:


- We doen ook veel werk rond large-scale machine learning, bijvoorbeeld in de context van high-throughput screening. Hierbij worden op zeer grote schaal beelden geanalyseerd (miljoenen beelden) en op deze resultaten (miljarden datapunten) machine learning toegepast om te voorspellen welke chemische stoffen potentieel hebben en verder geanalyseerd moeten worden. Onderzoeksvragen in deze context zijn bijvoorbeeld: “hoe kunnen we op een efficiënte manier een schaalbare, gedistribueerde beeldverwerking-pipeline opzetten als alternatief voor CellProfiler (http://cellprofiler.org)” Of ook: “een vergelijkende studie van large scale machine learning technieken voor high-throughput screening.”

Uitwerking
De exacte uitwerking zal uiteraard afhangen van het gekozen doel. Omdat zowel het domein van high-performance computing als life sciences nieuw zijn voorzien we inwerktijd. Het zal echter vrijwel altijd de volgende fases omhelzen:
• literatuurstudie: gedistribueerd programmeren, load balancing, DNA/RNA sequencing, vectorisatie, machine learning algoritmes, …
• uitwerken van een kern-oplossing, bijvoorbeeld een nieuwe efficientere sequence alignment aanpak, schaalbare visualisaties, …
• evaluatie van de oplossing(en), bijvoorbeeld een implementatie van de kern-oplossing en benchmarks om de performantie of kwaliteit van de resultaten te vergelijken met andere oplossingen.
• rapport dat de oplossing(en) voorstelt en evalueert op een wetenschappelijke manier.

Relevante literatuur
Referenties van sommige technieken werden gegeven in de tekst en worden verder gegeven afhankelijk van het gekozen voorstel.

Profiel
Implementeren schrikt je niet af: de kans is erg groot dat je je voorstel zal moeten implementeren en vergelijken met andere aanpakken.
Een open geest: je krijgt de kans (al is het geen verplichting) om te participeren in een zeer dynamische en brede context en contact te hebben met mensen uit de onderzoeks- en industriële wereld.

Type of project: Internship project

Degree: Master in Sciences or Master in Engineering majoring in computer science

Responsible scientist(s):
For further information or for application, please contact Roel Wuyts (roel.wuyts@imec.be).

Antigen – antibody interactions for surface-based biosensors

The specificity and affinity of antibody-antigen interactions are fundamental for understanding biological activity. Similar as other protein-protein interactions, they are non-covalent and reversible, formed by a combination of hydrogen bonds, hydrophobic interactions, electrostatic and van der Waals forces, and they may be significantly different on a surface compared to a reaction in solution. Studying these interactions are of highest importance in a vast number of areas of biomedicine and biotechnology.
To examine antibody-antigen pairing, different assays as well as label-free sensing technologies are available at imec. These latter technologies include both in-house systems (e.g. optical waveguide based sensing) as well as commercial devices (e.g. surface plasmon resonance based sensing using Biacore). Hence, the aim of this thesis is to study antigen-antibody interactions in detail using label-free methods as well as more traditional enzymatic (ELISA) and fluorescent assays.
More specifically, the overall affinity (described by the affinity constant KA) and kinetic parameters (kon and koff) of different antibodies will be determined for different conditions and sensor surfaces. As KA values vary widely for antibodies from below 105 M\(^{-1}\) to above 1012 M\(^{-1}\), the main goal of this thesis is to characterize and further understand antibody interactions on sensor surfaces. Better understanding in such surface interactions will assist biosensor development, especially for enabling rapid diagnostic tests. To bring this goal to a success, assays will be performed in imec’s biolabs and will be combined with in depth data analysis, including simulations and optimization and verification of different data fitting models.

Type of project: Internship and/or thesis project

Degree: Master in Sciences or Master in Engineering majoring in bio-engineering, nanoscience/nanotechnology
Responsible scientist(s):
For further information or for application, please contact Tim Stakenborg (tim.stakenborg@imec.be) and Wim Van Roy (wim.vanroy@imec.be).

**On-chip development of a fast, multiplex PCR assay**

Imec is a renowned center of excellence in the field of nano-electronics. Combining this expertise with life sciences results in novel opportunities, specifically in the field of point-of-care diagnostics. To enable DNA and RNA tests on a miniature platform, our team at imec has explored PCR on chip. Our current PCR chips have a small thermal mass enabling fast temperature cycling. Using these chips, PCRs have been performed in less than 10 minutes, but we envision that amplification times can be further reduced (to 5 min or less) by further optimization. In addition, quantitative PCR (qPCR) and even digital droplet PCR (ddPCR) have been performed on similar chips. qPCR is the most widely used standard tool for DNA and RNA detection, whereas ddPCR is a more recent developed technique which shows greater precision as well as less day-to-day variation.

During this master thesis, we aim to develop PCR multiplex assays on chip. This involves assay optimization both on standard bench-top tools as well as on-chip. Also optimization towards faster cycling time will be evaluated. Different techniques involving primer design, testing and evaluating the influence of different PCR components, microfluidic handling and analyzing the fluorescent detection system will be addressed.

**Type of project:** Internship and/or thesis project

**Degree:** Master in Sciences or Master in Engineering majoring in bio-engineering, nanoscience/nanotechnology, biomedicine, biochemistry

Responsible scientist(s):
For further information or for application, please contact Qing Cai (qing.cai@imec.be).

**Patterning of self-assembled monolayers for local functionalization of biosensor devices**

Biosensor devices are revolutionizing modern health-care as they enable to detect disease markers (e.g. protein biomarkers) in clinical samples. In integrated and miniaturized systems, also called lab-on-chip devices, the biosensor or transducer is part of a microfluidic platform that allows for a rapid and automated in-flow detection of the analyte. To ensure optimal sensitivity, a site-selective coupling of the bio-recognition molecules or receptors on the sensor area is required, while preferably the other areas (e.g. channel walls and non-sensing areas) must display non-adhesive properties to avoid any loss of the analyte.

At imec, we have explored different surface chemistries, mainly self-assembled monolayers of organosilanes, to ensure a covalent binding of the receptors to various biosensor devices. Using such optimized chemistries in combination with available lithographic technologies, site specific biofunctionalization strategies will be explored on a wafer scale to realize robust and reliable biosensor surfaces for multi-analyte detection. In this thesis, a specific aim will be to combine spotting technologies with microfluidic chip technologies to enable the site-specific immobilisation of antibodies in small microchannels. The obtained functional patterns will be characterized with different analytical techniques (e.g. contact angle goniometry, ellipsometry, XPS, etc.). Finally, the binding of biomolecules will be evaluated on the patterned interfaces. This research will lead to a low cost and high-throughput micro-patterning procedure that can be easily integrated in the manufacturing cycle of microfluidic based sensor device.

**Type of project:** Internship and/or thesis project

**Degree:** Master in Sciences or Master in Engineering majoring in chemistry, bio-engineering
Responsible scientist(s):
For further information or for application, please contact Rita Vos (Rita.Vos@imec.be).

Development of a high density DNA array using electrochemically induced reactions

Biosensor devices are revolutionizing modern healthcare as they enable to analyze clinical samples and to detect disease markers. To ensure optimal sensitivity combined with multiplex detection, a site-specific coupling of biomolecules on the sensor area is required.

At imec, we have explored different surface chemistries, mainly self-assembled monolayers of organosilanes, to ensure a covalent binding of the receptors to various biosensor sites. For electrochemical biosensors, we are developing a dedicated CMOS chip including individually addressable electrodes to electrochemically induce site-specific coupling reactions on these electrodes. The ultimate goal of this project is to fabricate high density DNA or protein arrays of unprecedented resolutions in-situ.

In this thesis, the specific aim will be to explore site-selective electrochemical reactions on the CMOS chip. More specifically, click reactions are envisioned to bind DNA molecules. Hereto, different electrochemical parameters will be characterized. Finally, the binding of DNA will be analyzed using different analytical techniques, e.g. contact angle measurements, cyclic voltammetry, TXRF. In short, this project will enable the fabrication of multiplex arrays that allow for low-cost biosensor integration in lab-on-a-chip systems by benefiting from CMOS scaling, ultimately resulting in truly innovative, high-end biological applications.

Type of project: Internship and/or thesis project

Degree: Master in Sciences or Master in Engineering majoring in bio-engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Karen Levrie (karen.levrie@imec.be).

Gratings for on-chip holography

Medical tests are increasingly being integrated in lab-on chip devices which can easily be used by physicians or patients. However, at the moment most integrated devices only check for chemicals, which severely limits the scope of these tests. Many routine medical tests, such as a complete blood count, rely on microscopy. At imec, we are trying to create a microscope of only a few cubic millimeters that can easily be integrated in a microfluidic system. Digital holography is an ideal imaging technique to scale down. Contrary to traditional microscopy, it does not require lenses and, since the image is formed in silico rather than physically, it requires very little space. Recently, we showed how white blood cells can be imaged with a compact holographic microscope, and how the obtained images can be used to perform a 3-part white blood cell differential, an important part of a complete blood count. Although our holographic device is considerably smaller than any normal compound microscope, it is not integrated yet.

To fully integrate our device, we need to create a high quality point source to illuminate the sample. For this, we are developing gratings which focusses light for an optical waveguide into a single point. Focusing gratings have used been for telecommunications, yet, the requirements for imaging are strongly different. In order to meet these requirements we are building up new models for complex gratings.

In this thesis, you will investigate scattering structures that can be implemented in our focusing gratings. Various metallic or dielectric scatterers will be simulated using optical design software to see how effectively and broadly they couple out light. After identifying a set of potentially good scatterers, the individual scatterers as well as gratings based on these scatterers will be fabricated on waveguides in order to measure their performance.
Active photonic control in silicon nitride

Several standard sensing and imaging methods in life sciences rely on the analysis of signals and patterns of light, by spatially measuring the intensity and/or the spectral content of transmitted, reflected, scattered or emitted photons. Often this requires the use of bulky and expensive optical instruments, limiting the use to specialized laboratories. Imec has been developing silicon nitride waveguide technology that allows to route and analyze visible light on a chip, seamlessly integrated with CMOS technologies. We have successfully demonstrated this technology already in a few applications, ranging from molecular sensing to spectroscopy.

A mature optical circuit also comprises switches, allowing selective excitation and sensing from specific sites. Infrared waveguide technology based on silicon photonics has a number of options for this, which tend not to work or to a much reduced degree in silicon nitride.

The purpose of this master thesis is to characterize the material in detail to reveal all relevant coefficients of the various mechanisms that can be used for active control. These include its thermal response, its nonlinear coefficients etc. In combination with extensive material characterization you will also design, fabricate and measure a specific implementation of an active component in integrated silicon nitride waveguides. The work involves literature study (25%), fabrication (25%) and optical characterization (50%).

Enhanced light-matter interactions mediated by plasmonic and photonic nanoresonators for optically detected magnetic resonance

Optically Detected Magnetic Resonance (ODMR) is a technique where a magnetic resonance in a material is detected optically by changes in the material’s luminescence intensity. Since the material’s magnetic resonance frequency depends linearly on an external magnetic field, ODMR in fact constitutes an optical magnetic field sensor.

One of the most prominent materials for ODMR is diamond containing paramagnetic spin defect centers. These centers act as unique atom-size magnetic field sensors that can be optically addressed and can operate at room temperature and ambient pressure. Ultimately leading to the development of nanoscale electron spin resonance (ESR) and nuclear magnetic resonance (NMR) spectroscopy and imaging under ambient conditions. This will enable label-free magnetic resonance sensing of individual electron or nuclear spins in complex biological systems. However, optical excitation and luminescence detection efficiencies are still limiting factors towards this end.
In our group we develop and investigate plasmonic and photonic resonators to enhance ODMR sensitivities. These metallic and dielectric nanostructures can convert free space light into highly localized fields, providing a very effective route to couple photons in and out of the nanoscale defect centers in diamond.

In this master thesis, the student will gain hands-on experience with sample preparation in the imec cleanroom, scanning electron microscopy (SEM), and optical experiments (in close collaboration with the KU Leuven Department of Physics). The experimental results will be verified and complemented by full-field 3D electromagnetic simulations.

**Type of project:** Thesis project

**Degree:** Master in Science and Master in Engineering majoring in physics, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Niels Verellen (Niels.Verellen@imec.be).

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**Lipid membranes studied at a single-molecule level using a nanophotonic platform**

Single-molecule (SM) methods provide a powerful way to investigate features that are usually obscured by ensemble averaging, such as transient subpopulations, enzyme dynamics and reaction mechanisms. Some of the most popular techniques employed to investigate single molecules are super-resolution fluorescence microscopy, electrophysiology with nanopores and atomic force microscopy. In recent years photonics and plasmonics, often in the form of nanostructured devices, have also been employed improve or combine these techniques.

Amongst the most interesting molecules to study are biopolymers, i.e. DNA or proteins, which form the most basic building blocks of life. The intricate details of their working mechanisms and their interactions with other molecules are of paramount importance in many fields, including medical science, development of biosensors and drug development. Proteins that associate with the cellular lipid bilayers, called membrane proteins, are particularly important since they mediate many vital functions ranging from signaling to the selective transport of molecules across the membrane. They constitute about 30% of the human proteins and represent about 60% of the drug targets. Studying single membrane proteins at a SM level in a physiologically relevant environment is not trivial however, and current technologies are heavily limited in their throughput or resolution. We therefore propose to develop a platform that enables the high-throughput, SM-level study of membrane protein systems. Such a device would consist of a nanostructured surface, coated with a phospholipid bilayer into which membrane proteins can be embedded.

In this master thesis, the student will learn how to fabricate nanostructures in the III-V area of the imec cleanroom using e-beam lithography under the guidance of the daily supervisor. (S)he will characterize them using optical and scanning electron microscopy. Simultaneously, the student will investigate how different surfaces can be coated with a planar lipid bilayer and study them with optical (fluorescence) microscopy and electrical measurements. Finally, both techniques will be combined into a single platform. The student will gain experience in (e-beam) lithography, various etching and thin-film deposition techniques and in the synthesis of lipid bilayers. (S)he should be interested in combining solid-state technology with biology and have an engineering mindset. The background can be either in (bio)chemistry or nanotechnology.

**Type of project:** Thesis project

**Degree:** Master in Science and Master in Engineering majoring in chemistry, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Kherim Willems (Kherim.Willems@imec.be).
**Nano-photonic structures to collect and enhance fluorescence emission on a SiN platform**

Silicon photonics has become one of the most promising photonic integration platforms at visible wavelengths in the recent years. The combination of high-index-contrast and compatibility with CMOS processing technology made it possible to use the electronics fabrication facilities to make photonic circuitry. There is a tremendous interest towards integration of photonic devices in biological sensing and detection. The visible and very-near-infrared (500-950 nm) wavelength window is of great interest for this kind of applications due to low photo damage and availability of low cost sources-detectors. Unlike Silicon (Si), Silicon Nitride (SiN) is transparent in this Visible & Near-Infrared window and provides the combination of high-index-contrast and compatibility with CMOS processing technology. A low-loss silicon nitride platform has been developed at IMEC’s 200 mm fab with propagation losses below 0.5 dB/cm in visible wavelength.

For ultimate integrated fluorescence based biosensing applications, the development of devices that efficiently both excite and collect fluorescence from dyes located near the chip surface is of paramount importance. In this work, the aim is to investigate the effect of different nano-photonic structures on the fluorescence emission of the dyes residing in the near field of the structures. This investigation will help to develop nano-photonic devices to enhance the fluorescence emission and collect that efficiently by the chip. The student will use FDTD simulation to optimize the design for structures like waveguides, ring resonators and linear resonators. Then (s)he will fabricate them using electron beam lithography. Finally, (s)he will investigate the influence of those structures on the fluorophore placed in the near field. The student will gain hands-on experience with optical experiments. Sample preparation will be handled by the student in the imec III-V cleanroom in cooperation with the daily advisor. The student will obtain experience in optical and electron beam lithography and master various deposition and etching techniques. Further sample characterization will be done by optical microscopy, scanning electron microscopy and waveguide transmission spectroscopy. The candidate should have a strong interest in photonics and nanofabrication.

**Type of project:** Thesis or thesis with internship project

**Degree:** Master in Science and Master in Engineering majoring in physics, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Md Mahmud-Ul-Hasan (Mahmud70@imec.be).

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**DNA detection assays on integrated photonic structures**

Since its introduction, the polymerase chain reaction (PCR) has become an indispensable tool in clinical diagnostics. In recent years, significant advancements emerged in the area of miniaturization of PCR using microfabricated structures with clear benefits. Not only the speed and the efficiency of the amplification were improved, also the assay costs are reduced by downscaling due the lower consumption of expensive reagents. Detection is traditionally done using fluorescence. If optical analysis is to be part of an integrated solution, all optical components should be miniaturized as well.

For this reason, in the last few years imec has developed a silicon nitride (SiN) photonics platform which operates in the visible and infrared region of the light spectrum. Various photonic structures such as grating couplers, waveguides and resonators have been designed, fabricated and characterized. The resulting microfabricated photonic circuits are now ready for performing various biological assays. The student will evaluate the performance of DNA detection assays on these silicon nitride photonic microstructures. The very nature of this research topic calls for a broad interest in both bio- and nanotechnology. The student will gain hands-on experience with several molecular biology techniques as well as the modification of different optical setups. For all aspects of this research topic, support is available in the teams of imec’s Life Science Technologies department.
Fluidic modeling and experimentation for high speed jet flow cell sorting

Cell sorting is a very important sample pretreatment step for many bio-analytical applications. Not only does it provide cell counts for different species in the crude sample, the sorted thus purified cell species are important for downstream diagnosis and therapy. For example, circulating tumor cells (CTCs) can be sorted out from other white blood cells (WBCs) for cell genotyping so as to guide personalized medication to stop cancer metastasis. Imec has developed a high speed cell sorter platform where cell sorting takes place in a microfluidic chip in contrast to bulky traditional bulky cell sorters. The key element of the cell sorter is a micro heating element which fires micro vapor bubbles and consequently a rapid jet flow that sorts cells. (Details can be found from: http://cyto.tinyfluidix.com/?p=162). The main focus of this thesis is to study the dynamic process of the vapor growth and jet flow mechanism by physical analysis and computer thermal/fluidic finite element modeling (70% of total time). The modeling will be cross verified by existing or new experimental data (30% of total time). The candidate background is preferably science (physics) or engineering.

PEDOT functionalization of neural probes for fluorescence labeling

Implantable silicon-based neural probes for high-density neural recordings and/or stimulation have made significant impact on society as tools for the investigation of brain function and for the development of neural prostheses. While great efforts have been made to develop new technologies, the understanding of how neural tissue responds to such invasive implants is lagging behind the technological development. Without this understanding it is very difficult to exactly pin down causes for the frequently observed deterioration of recorded signals or stimulation efficacy over time. To gain insight in such processes, it has become clear that a multimodal approach is mandatory.
For this project, we want to functionalize imec probes by depositing PEDOT:PSS on the electrode contacts. The student will develop a protocol and tune parameters for electrodeposition of PEDOT:PSS starting from existing recipes and literature and develop a procedure to incorporate fluorescent agents that are stable on the shelf and in vivo for several days. This project involves chemical preparations, electrodeposition, impedance measurements, and microscopy to qualitatively and quantitatively verify the electrodeposition process. The candidate ideally has theoretical and practical knowledge of electrochemistry is able to work independently.

Type of project: Internship project

Degree: Master in Science majoring in chemistry, materials engineering, bio-engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Katrien Mols (Katrien.Mols@imec.be) and Silke Musa (Silke.Musa@imec.be).

Impedance sensing of bacterial biofilms

Bacterial biofilms are complex surface-associated communities of microorganisms embedded in a self-produced matrix. Within a biofilm, bacteria are up to 100 times more tolerant to antibiotics and disinfectants. As a consequence, biofilms cause very persistent contaminations and infections. Nowadays, there is a strong need for in-situ detection techniques, e.g. on implants, on catheters, or in industrial piping systems, that would reduce the costs that biofilm formation causes. At imec, we are developing microelectrode-based electrochemical impedance sensors that allow for in-vivo biofilm monitoring.

This project aims to develop an impedance sensing assay to detect and characterize bacterial biofilm formation using different CMOS chips. To achieve this goal, the student will (i) develop software improvements in our biosensing platform, (ii) optimize the protocol for the impedance sensing assay and (iii) provide an electrical model for the bacterial biofilm.

The candidate should have experience in electrical modeling, measurement techniques and software programming (Matlab, C-Sharp).

Type of project: Thesis and/or internship project

Degree: Master in Engineering majoring in physics, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Dries Braeken (Dries.Braeken@imec.be).

Development of motion vector algorithms for the evaluation drug cardiotoxicity in cardiac contractile behavior

Cardiotoxicity is the major cause of drug withdrawal from the market, despite rigorous toxicity testing during the drug development process. Existing safety screening techniques (optical, impedance, cellular assays) are either too limited in throughput or offer too poor predictability of toxicity to be applied on large numbers of compounds in the early stage of drug development. As a result, imec has developed a compact optical system for direct monitoring of fast cellular movements that enable low cost and high throughput drug screening based on high-speed lens-free in-line holographic microscope. Holograms obtained by lens-free imaging are then analyzed through motion vector algorithms to extract parameters related to contractility and give insight into the action of drugs on cardiac cells.
The focus of this project is the development of software that evaluates the effect of certain drugs on cardiac monolayers by analyzing the physical contraction of cardiomyocytes. By developing scripts based on optical flow, parameters related to both cardiac contractility and the transmission of excitation waves through the cardiac monolayer will be extracted from unprocessed holograms. These algorithms will then be evaluated on a series of drugs which affect the strength of contraction. So, the candidate should have a good background and understanding of image processing, data analysis, and software development (Matlab, Python).

**Type of project:** Thesis and/or internship project

**Degree:** Master in Industrial Sciences and Master in Engineering majoring in physics, electrotechnics/electrical engineering

**Responsible scientist(s):**
For further information or for application, please contact Thomas Pauwelyn (Thomas.Pauwelyn@imec.be) and Dries Braeken (Dries.Braeken@imec.be).

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**Cancer cell classification using spectroscopy**

Conventionally, immunocytochemistry is used for single cell identification. This process relies on a specific interaction between an antibody and antigen and involves incubation of the sample with an antibody solution. Often the cells are not viable after the identification process and can’t be used for further molecular analysis. Raman scattering is an optical spectroscopy method that allows to differentiate chemical biomolecules based on their vibrational or rotational modes. This method doesn’t alter the native cell state and elaborate preprocessing of the sample is not necessary. Differences has been shown in Raman spectra of different cell types. The purpose of this thesis is to do a statistically relevant study on the potential of Raman spectroscopy to distinguish several cancer cell types. Data analysis is crucial for success of this technique, as differences between the spectra are very small. Principal component analysis is currently used to extract the most important differences. In literature principal component analysis and linear discriminant analysis are combined in order to distinguish between cell types. Data preprocessing and classification algorithms are implemented in MATLAB.

**Type of project:** Thesis project

**Degree:** Master degree

**Responsible scientist(s):**
For further information or for application, please contact Evelien Mathieu (Evelien.Mathieu@imec.be) and Pol van Dorpe (pol.vandorpe@imec.be).
V. Wireless Communication

High speed and reliable digital design for wireless communication

As the demand of the transformation towards 4/5G telecommunication network, multiple standards are trying to push their throughput higher towards Gbps. The design of high speed DSP blocks with low power consumption is becoming essential in baseband design for wireless receiver. The CMOS technology scaling towards sub 20 nm definitely helps to make the digital circuit run faster at low supply voltage hence low power consumption, however we would like to explore methods to increase the throughput of DSP blocks (especially in channel coding/decoding) from algorithm and architecture level further. The applicant should have digital signal processing (knowledge on channel coding, such as Turbo, LDPC codes will be a plus) and digital circuit design background. Better to be familiar with digital design flow from RTL modeling to synthesis with back end experience will be a plus.

Type of project: Thesis with internship project
Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Andre Bourdoux (Andre.Bourdoux@imec.be), Meng Li (Meng.li@imec.be) and Yanxiang Huang (Yanxiang.huang@imec.be).

60GHz communication prototyping on a fast FPGA platform

Communications at 60GHz is an emerging communication technology that has recently been standardized (IEEE802.11ad/WiGig) for fast market adoption. Future standards will probably emerge in a near future, with enhancements and more features. We have developed such a 60GHz communications chip at imec, integrating all the RF and analog hardware including beamforming capability. The goal of this thesis is to implement transmitter and receiver signal processing algorithms on an advanced FPGA platform that will be interfaced with the imec 60GHz chip for performance evaluation and experimentation. The challenge resides in the very high speed of the signal processing, requiring careful architectural choices and parallelization. Additionally, the system requires high-speed connectivity to a PC combined with a software application that performs data post-processing and provides graphical output. The applicant must have a sound understanding of digital signal processing. He/She must have a good background in digital circuit design (VHDL) and also have some experience with Matlab. Knowledge of digital communications principles, software development (C/C++) and Linux OS is a plus.

Type of project: Thesis or thesis with internship project
Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Andy Dewilde (Andy.Dewilde@imec.be) and Andre Bourdoux (Andre.Bourdoux@imec.be).
Radar sensors have long been used in defense and security applications. They were bulky, costly and power hungry. Today, radar sensors can be implemented in a single-chip, in a cheap CMOS process, opening up many consumer and automotive applications. We have developed such a chip at IMEC targeting applications such as automotive radars, robotics and smart cities/smart building. The chip integrates all the 79GHz RF and analog hardware and the first stage of the digital processing.

The goal of this thesis is to further implement the signal processing algorithms on an advanced FPGA platform that will be interfaced with the IMEC 79GHz chip for performance evaluation and experimentation. The challenge resides in the very high speed of the signal processing, requiring careful architectural choices and parallelization. Additionally, the system requires high-speed connectivity to a PC, combined with a software application that performs data post-processing and provides graphical outputs.

The applicant must have a sound understanding of digital signal processing. He/She must have a good background in digital circuit design (VHDL) and must also have some experience with Matlab. Knowledge of radar principles, software development (C/C++) and Linux OS is a plus.

Type of project: Thesis or thesis with internship project

Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Andy Dewilde (Andy.Dewilde@imec.be) and Andre Bourdoux (Andre.Bourdoux@imec.be).
VI. Image Sensors and Vision Systems

A Low-Dropout regulator for CMOS image sensors

Imagine a pocket-size blood analysis device, providing you with an early warning that cancer is spreading in your body. Advances in imager technology will enable such exciting concepts and applications. So far, CMOS image sensors have been providing increased functionality and performance, and replaced the analog CCD solutions in many applications. Lower cost and power have supported common deployment in mobile devices. Sensors now allow analysis of many thousands of images per second, and new applications are enabled by more integrated functionality and more data provided by these sensors.

Imec develops specialty image sensors to enable new frontiers in imaging. With increased sensor speed and resolution increasing as well, the requirements on the circuit are very challenging. One of these challenges is to develop a stable supply voltage. Image sensors typically contain thousands of ADCs (Analog to digital converters) polluting the supply voltage, creating coupling, being sensitive to temperature and voltage. The challenge is to create a regulator for these thousands of ADCs in very large sensors chip, over a large area.

This thesis will start with a literature survey and targets finalizing a silicon design and layout of an LDO (Low Dropout Regulator) for these applications.

**Type of project:** Thesis project

**Degree:** Master in Engineering majoring in electrotechnics/electrical engineering

**Responsible scientist(s):**
For further information or for application, please contact Jonathan Borremans (Jonathan.Borremans@imec.be), David San Segundo Bello (David.SanSegundoBello@imec.be) and Jean-Luc Bacq (Jean-Luc.Bacq@imec.be).
VII. Large Area Flexible Electronics

Growth of highly ordered organic semiconductors

P-type thin film transistors (TFT) based on latest generation organic semiconductors (\( \text{C}_8\)-BTBT, \( \text{C}_{10}\)-DNTT) display excellent characteristics, with charge transport mobility of up to 10 cm\(^2\)/Vs. These materials reach the quality levels of n-type oxide semiconductors (IGZO), potentially enabling the development of a complementary technology (CMOS) for low-cost electronic circuits on large area flexible foils. Examples of potential applications for such circuits are RFID tags, smart packaging, flexible displays and numerous biomedical applications.

Among other things, the performance of organic TFT depends on the degree of crystallinity of the organic semiconductors. Higher ordering delivers better performance, and, the best TFTs are based on defect free single organic crystals. The production of thin films of defect free organic single crystals over large area is therefore highly desirable. This, however, remains a considerable challenge since the presence of only a few defects will negatively impact the spread of TFT characteristics. As the spread increases, the yield of circuits dramatically decreases.

In this internship we propose to work on the development of techniques to achieve the growth of highly ordered organic semiconductor, following two routes. A first route is the development of substrate treatments that help to template the growth of organic-semiconductors and increase their degree of order. Templating, that relies on a good match between the crystal structures of the substrate and the grown material, is very well known in the field of epitaxial growth of inorganic materials. In the field of organic, however, much remains to be done. A second route is the optimization of the semiconductor growth technique, either from solution or from vapor. Achieving a high degree of order requires a spatial separation of the crystal nucleation event and the subsequent crystal growth. This is best achieved in a system involving linear motion that pulls a growing front.

The work is mainly experimental and will include substrate preparation and treatment, organic semiconductor deposition, either from the vapor phase or from a solution, and the fabrication of TFTs to characterize the electrical properties of the templated layers.

Objective for imec
- Explore the potential of substrate treatments to template the growth of high performance organic semiconductors and achieve a better ordering
- Optimize our highly ordered organic semiconductor fabrication technologies

Objective for the candidate
- Learn fabrication techniques that are relevant in microelectronics
- Learn basics of crystal growth and TFT characterization
- Learn the design of experiments
- Work as a team in a professional research environment

Skills required
- Material science background
- Knowledge in electronics
- Handy in the lab
- Self-motivated and independent hard worker

Type of project: Thesis with internship project

Degree: Master in Science and Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Cédric Rolin (Cedric.Rolin@imec.be).
Organic patterning

The ever-increasing resolution of displays and imagers fabricated using organic semiconductors requires new, advanced patterning techniques. Currently, the most popular fabrication process for high-resolution displays based on thermally-evaporated OLED stacks is shadow-masking. Still, this technology has limitations in terms of the smallest feature size and up-scalability for very large substrate sizes. As an alternative, dedicated photolithography processes can be used. In this case, special care needs to be taken to ensure chemical compatibility of the processing products used with the very fragile organic compounds. Imec is active in developing novel solutions enabling patterning of advanced organic semiconductor devices by photolithography. The focus of this internship will be optimization of the fabrication process of high-resolution organic photodetectors and light emitting diodes. Active layers will be deposited by spin-coating (solution processed polymers) or thermal evaporation (evaporated small molecules). The student will be involved in the entire fabrication cycle, performed in the state-of-the-art facilities including imec’s cleanroom and dedicated organic line. Initially, the student will receive training on the relevant processing and characterization tools. After a short introduction to the facilities, an independent investigation is expected with the focus on short-term research goals. As this internship is focused on the photolithography aspects of the semiconductor fabrication route, experience in this domain is a necessity. The minimum duration of the internship is 6 months.

Type of project: Internship project

Degree: Master in Industrial Science and Master in Science and Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Pawel Malinowski (Pawel.Malinowski@imec.be) and Tung Huei Ke (Tung.Huei.Ke@imec.be).

Organic photodetectors

Organic semiconductors are used in many fields of photonics. Displays fabricated using organic light emitting diodes (OLED) can be found in modern smartphones and tablets, whereas organic solar cells (OPV - organic photovoltaics) are emerging with demonstrated efficiencies above 10%. Organic photodetectors (OPD) are another very interesting domain, with ultrathin active layers (order of tens of nanometers) providing performance comparable to bulk inorganic devices. Thanks to a multitude of possible compounds, parameters such as response spectrum, cut-off wavelength etc. can be easily tuned. Because of very high absorption coefficient and low refractive index, issues such as reflection or crosstalk can be minimized. Another exciting feature is the low processing temperature and thus feasibility of using a flexible foil as substrate, leading to rollable or curved photodetector arrays.

The focus of this internship will be optimization of the fabrication process of advanced organic photodetectors and investigation of their performance with respect to industrial specifications. Active layers will be deposited by spin-coating (solution processed polymers) or thermal evaporation (evaporated small molecules).

The student will be involved in the entire fabrication cycle, performed in the state-of-the-art facilities including imec’s cleanroom and dedicated organic line. Initially, the student will receive training on the relevant processing and characterization tools. After a short introduction to the facilities, an independent investigation is expected with the focus on short-term research goals. Internship of at least 6 months is required.

Type of project: Thesis and/or internship project

Degree: Master in Industrial Science and Master in Science and Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Pawel Malinowski (Pawel.Malinowski@imec.be).
Organic light emitting diode (OLED) with high stability

Organic light emitting diode (OLED) is the most well-known organic electronics in the display and lighting industry. It is lightweight, low power, with wide viewing angle and fast response time, which is very promising for the display of portable electronics. Furthermore, it can be integrated with flexible back-plane panel for flexible active matrix OLEDs (AMOLEDs) display. For OLED device, it is very sensitive to ambient environment, especially water and oxygen. It is necessary to develop stable OLED stacks for various process conditions. The goal of this internship is to develop a stable OLEDs stack with good device performance for different applications.

Task description:
1. Development of highly thermal stable OLED stack for long hour heating treatment: Organic semiconductors with high thermal stability will be evaluated in OLED devices. The developed OLED stacks will be applied in a back-plane panel with thin-film encapsulation for demonstration of flexible AMOLED display.
2. Study the impacts of all kinds of process on the OLEDs stacks. Different measurements including photophysical properties like PL and PLQY or excited state lifetime and device reliability tests would be investigated. The minimum duration of the internship is 3 months. Six months is preferred.

Type of project: Internship project

Degree: Master in Industrial Science and Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology, energy

Responsible scientist(s):
For further information or for application, please contact TungHuei Ke (Tung.Huei.Ke@imec.be).

High speed data acquisition for real-time X-ray detector

Large-area image sensors are traditionally made using hydrogenated amorphous silicon (a-Si:H) thin-film transistors and diodes as the select/switching element and photosensitive element respectively. However large-area image sensors processed on thin film plastic foils would be lighter and less fragile than current glass-based designs. Mechanical flexibility offers unique prospects for highly innovative product designs, concepts, and applications. For example, combined with an X-ray phosphor screen, it will allow the construction of flexible image sensor for digital radiography, reducing the discomfort caused by the rigid flat panel sensors in intraoral radiography. New readout and compensation solutions are needed to readout the image sensor with thin film transistors. The goal of this internship is to investigate the different options to read out the sensor and process high speed image data. Different hardware/software solutions will be developed and performance will be benchmarked.

Requirements:
- Self-motivated and independent
- Experience in C/C++ embedded software development
- Knowledge of the VHDL programming language
- Experience in digital and analog circuit design for printed circuit boards (PCBs).
- Experience with bench level test and debug of electronics.

Type of project: Internship project of 3 to 6 months

Degree: Master in Industrial Science and Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Ameys Marc (Ameys.Marc@imec.be).
Multiplexed driving of an AMOLED display

AMOLED displays start to gain a lot of popularity in the display industry. They are light-weight, low power, with wide viewing angle and fast response time, which is very promising for the display of portable electronics. The signal wiring of these displays becomes more and more a challenge due to the higher DPI. The goal of this internship is to build an AMOLED display driver setup that works with multiplexed data lines.

Requirements:
- Self-motivated and independent
- Experience in C/C++ embedded software development
- Knowledge of the VHDL programming language
- Experience in digital and analog circuit design for printed circuit boards (PCBs).
- Experience with bench level test and debug of electronics.

Type of project: Internship project of 3 to 6 months

Degree: Master in Industrial Sciences and Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Ameys Marc (Ameys.Marc@imec.be).

Integration of a charge-trap layer with a-IGZO active channel for nonvolatile memory transistors

In recent years, amorphous oxide semiconductors (AOSs) are of great interest for thin-film transistor (TFT) channel layer applications. They have been studied due to their superior characteristics, such as high uniformity, high electron mobility between 10-50 cm²/V·s, and their fabrication at low temperatures on plastic substrates. These advantages of a-IGZO thin-film transistors are promising for next-generation backplanes for displays and circuits on transparent and flexible substrate. In transparent and flexible system applications, nonvolatile memory devices are also essential components. Oxide-based Charge-Trap Memory (CTM) can be a promising candidate for this field owing to the low temperature process compatibility of oxide semiconductor materials. In the published work, the realization of oxide CTM with the various charge-trap (CT) layers such as nanoparticles (Pt, Au, and Ag), dielectrics (SiOx, Si3N4, and Al2O3), and oxide semiconductors (ZnO) have been explored. However, the issues of program speed and retention time need to be improved. The gate-stack design, materials and their thickness plays important role on these characteristics.

The objective of this Master thesis/internship is to integrate a charge-trap layer in our top gate a-IGZO TFT stack. Excellent nonvolatile memory characteristics of the proposed CTMs are expected. From the results a conclusion need to be drawn on the device structure, interface issues & material of the charge trap layer. This activity also includes the measurements of the manufactured devices. If time allows, the student will also investigate the devices on the flexible substrates.

Type of project: Internship of thesis with internship project

Degree: Master in Science and Master in Engineering majoring in physics, materials engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Manoj Nag (Manoj Nag@imec.be) and Florian De Roose (florian.de.roose@esat.kuleuven.be).
Design environment and design flows for thin film technologies

Large area electronics are getting more and more attention over the last years, ever since the discovery of new high-performing thin-film semiconductors like a-IGZO. These new semiconductors have a factor 10 to 100 more mobility and allow for integration of the circuits on a flexible circuits. Therefore there has been an incredible boom in the number of applications, going from low cost packaging tags to flexible displays. There are, however, a great number of applications which cannot efficiently be explored due to the lack of design tools tailored for this novel technology. During this internship you will improve the quality of the design flow in order to unlock more advanced applications.

In order to advance the circuit design in this technology, we essentially require a qualitative Process Design Kit (PDK). For analog design, this includes the possibility to do a Design Rule Check (DRC), a netlist extract (PEX) and finally a Layout vs Schematic (LVS) check. Ideally PCells and standardized blocks are part of this analog design kit, so as to increase design speed.

Furthermore we want to implement an advanced digital design flow to improve both the efficiency of implementation in terms of area and speed and the quality of the resulting circuits. A flow for doing a place-and-route with digital standard cells should be further developed.

You, as a student, will incrementally improve the design environment and design flow for thin-film technologies, starting from the analog design, working up to the standard cell and place-and-route tools. You have the opportunity to work in a world-class design group in thin-film electronics, with the prospect of your results being used for the years to come.

Requirements:
- Self-motivated, inquisitive and independent
- Experience in Linux and Cadence
- Capable of writing clear reports

Type of project: Internship project of 3 to 6 months

Degree: Master in Industrial Sciences and Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Florian De Roose (Florian.DeRoose@imec.be) or Nikolaos Papadopoulos (Nikolas.Papadopoulos@imec.be).
VIII. Solar Cells and Batteries

Development and characterization of high band-gap thin films for use in solar cells

Today, record single-junction solar cell efficiencies are approaching their theoretical limit of 30% under 1-sun illumination. One method to increase efficiency even further is the development of tandem solar cells. A tandem solar cell consists of two cells: a high band-gap cell (1.5-2.0 eV) harvests the high-energy photons and a lower band-gap cell (1.0-1.5 eV) harvests the low-energy photons. This approach leads to theoretical efficiencies of 44% under 1-sun illumination. However, tandem solar cell development has been mainly focused on costly materials; and is not yet feasible at low-cost as there is no stable and abundant high band-gap top cell alternative demonstrated. See [1,2]. For that reason the thin film (TF) solar cell group in Imec studies novel high band-gap TF materials with potential to be low-cost. Within this group, TF materials based on the Cu2ZnSn(S,Se)4 (CZTSSe) material system are developed and characterized, but also tested in actual solar cells. The aim is to enhance the scientific understanding of these materials and to develop novel solar cell technologies. This study started in 2011 with the development of pure selenide sputtered CZTSe thin films; wherefore a state-of-the-art top efficiency of 10.4% has been obtained. More recently, also CZTGeSSe (and CZTSiSSe) TF materials are developed and studied; early research indicating that substitution of Sn with Ge (resp. Si) in the CZTSSe crystal lattice leads to an increase in band-gap and enhanced material quality. See [3,4].

This study of similar and other interesting high band-gap TF candidates remains at the forefront of TF solar cell research, where physicists, engineers and chemists have the ability to successfully contribute. So, if you are interested in this work, then please contact the supervising scientist to find out if your profile fits this research.


Type of project: Thesis or/and internship project

Degree: Master in Sciences or Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering, energy, nanoscience/nanotechnology

Responsible scientist:
For further information or for application, please contact Bart Vermang (Bart.Vermang@imec.be).

Optoelectronic characterization of Kesterite solar cells

Next to Si-based solar cells, devices based on chalcogenide thin films, such as CdTe and Cu(In,Ga)(Se,S)2 (CIGS), are at the forefront in thin film solar cell technology. However, reliance on the heavy metal Cd and on the non-abundant elements In and Te presents a major barrier towards meeting the multi-terawatt-scale target for renewable energy supplied by photovoltaics. Moreover, thin film PV has to compete with present efficiencies of silicon solar cells above 20%. Therefore, multi-junction PV solutions will be needed in the future.

Kesterite CZT(S,Se) or CZSi(S,Se) is an emerging alternative chalcogenide solar cell absorber that provides diversification away from the non-earth-abundant elements mentioned above and has the promise of the development of a multi-junction TF solar cell. Depending on the exact stoichiometry and choice of the different elements in the absorber, the band gap of the absorber can be varied between 1 and 2 eV, which makes the combination of different absorbers into multi-junction thin film solar cells or multi-junction thin film Kesterite-Si solar cells possible.
This master thesis topic consists of electrical and optical characterization of Kesterite films and solar cells. Electrical measurements to be performed consist of current-voltage and capacitance-voltage measurements of Kesterite solar cell structures. All measurements will be performed as a function of temperature and illumination intensity, in order to fully characterize the diode parameters of the solar cell structure and to gain insight into the dominant recombination processes in the cell.

Optical measurements to be performed consist of temperature and intensity dependent photoluminescence and time-resolved photoluminescence measurements. These measurements will allow further insight into the different recombination mechanisms in the solar cells. The different characterizations will be linked to the growth of the absorber in order to optimize the absorber quality for solar cell applications.

**Type of project:** Thesis or internship project

**Degree:** Master in Sciences or Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, energy, nanoscience/nanotechnology

**Responsible scientist:**
For further information or for application, please contact Guy Brammertz (brammert@imec.be).

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**Optimization of the porosification of silicon for application in thin-film crystalline silicon solar cells**

Thanks to its peculiar properties, porous silicon has been extensively employed in different fields of science and technology, from MEMS technology to biosensors. Within silicon solar cells technology, porous silicon layers can fulfill various functions, such as those of light reflector or anti-reflector, sacrificial layer for patterning, or structure-weakening layer. At imec, we are developing an advanced process for thin solar cells in which porous silicon plays a double and key role: first, as seed layer it enables the growth of a high-quality thin film (few tens of micrometers) of silicon, and second, as weakening layer it enables the detachment of this film for transfer onto a low-cost substrate. The object of this research topic is to optimize the fabrication of this porous layer in order to improve the reproducibility of the process.

Fabrication of porous silicon is done by electrochemical etching (anodization) of a highly-doped silicon substrate. The etching process takes place in a solution containing water, HF and an alcohol. The porosity of the layer, a crucial property for detachment, is determined by processing parameters like the anodization current density and the electrolyte composition (cf. the figure below, where a double layer of low and high porosities was successively grown). But other secondary parameters, such as temperature or metal contamination can also impact the porous layer quality. Your task will be to investigate the impact of various parameters on the detachment yield of the silicon films, identify which ones are essential for our process, and gain control on them. This work will be experimental and will take place at a wetbench, in cleanroom environment. For this application you should therefore have a hands-on attitude and be cautious. A background in semiconductor sciences and/or (electro)chemistry is preferred.

**Type of project:** Thesis with internship project

**Degree:** Master in Sciences or Master in Engineering majoring in chemistry, materials engineering, energy, nanoscience/nanotechnology

**Responsible scientist:**
For further information or for application, please contact Valerie Depauw (valerie.depauw@imec.be) and Kris Van Nieuwenhuysen (vnieuwen@imec.be).
Silicon epitaxy as doping technology in bulk crystalline silicon solar cells: modelling of the recombination losses as a function of doping profile and passivation

The general PV strategy of imec focuses on the reduction of silicon usage, the increase of cell efficiency and the simplification of the solar cell process flow, that is, overall, the decrease of the cost per Watt peak for solar energy production. The research and development (R&D) on advanced doping process technologies is one of the routes followed at imec to accelerate the growth of silicon solar cells in a sustainable way; and selective epitaxial growth (SEG) is one of those technologies under investigation as potential alternative to surpass standard diffusion for the application of local doping. Two main platforms based on n-type crystalline silicon are used at imec for the integration and benchmark in an industrial process flow of epitaxy: IBC (interdigitated back contact) and PERT (passivated emitter and rear totally diffused) solar cells (see Figure 1).

At imec, the integration of a p-type epitaxial emitter in both IBC and PERT solar cells allows a significant simplification of the cell fabrication flow compared to the baseline sequence which relies on BBr₃ diffusion. The integration of a p-type epitaxial emitter in these platforms already demonstrated efficiencies up to 22.8 % and 21.5 % in IBC and PERT cells, respectively. Besides, the potential to further simplify and improve the device performance has also led to initiate a new activity to introduce an n-type local BSF by SEG in IBC cells.

In order to further exploit the large degree of flexibility in epitaxy to design a doped profile in one-step process, an extensive investigation has been realized to develop the suitable process conditions for the growth of new advanced profiles (ultra-shallow profiles, 2-step profiles, exponential-like profiles...).

The research work where the topic of the Master/Internship student will be integrated consists of the physical and electrical characterization of doped regions grown by selective silicon epitaxy, aiming at the screening of the most suitable profiles for our applications. The activity of the Master/Internship student will focus on the use of computer simulation programs such as Quokka from PV Lighthouse or Sentaurus TCAD from Synopsys to evaluate and predict the recombination losses in these regions in the following terms:

- Dark saturation current density (Jₒ) and surface recombination velocity (S) for n-type and p-type epitaxial profiles, and benchmarking with experimental results.
- Evaluation of the impact of Auger recombination versus surface recombination as a function of the properties of the epitaxial profile and the properties of the dielectric(s) used for passivation (main focus on PECVD SiOₓ and ALD Al₂O₃).

**Figure 1:** Schematics of imec’s n-type IBC and PERT solar cells integrating doped regions grown by SEG

**Type of project:** Thesis with internship project

**Degree:** Master in Engineering majoring in physics, materials engineering, eletrotechnics/electrical engineering, nanoscience/nanotechnology
Characterization of carrier selective contacts using polysilicon-based structures

In order to approach the thermodynamic efficiency limit of silicon solar cells, commonly termed the Shockley-Queisser limit, the high-efficiency silicon devices aim at the implementation of structures which can suppress the recombination at the metal-semiconductor contacts to achieve the maximum open circuit voltage. An approach which shows high potential to minimize minority carrier recombination in those regions enabling an efficient majority carrier transport and collection is the concept of ‘carrier selective contact’ for which a general schematic is depicted in Figure 1.

In a silicon solar cell there are several options to design a ‘carrier selective contact’ structure depending on the nature and properties of the different layers – for example, polysilicon, SIPOS (Semi-Insulating POLycrystalline Silicon), amorphous silicon... as the so-called “membrane” on top of a thin-layer of chemical oxide, thermal oxide, intrinsic amorphous silicon... as the so-called “interfacial layer” –. One of the alternatives investigated at imec to implement this approach in our n-type PERT and IBC solar cell platforms relies on the growth of polysilicon contacts on chemical oxide.

With the goal of not increasing the process complexity in terms of number of steps and significant modification of the present cell process sequences, the research work where the Master/Internship student will be integrated focuses on the deposition by LPCVD of in-situ doped silicon layers on surfaces covered by a chemical oxide coming from the prior cleaning to deposition. Taking into account the synergies between both platforms regarding the boron doped emitter-aluminium contact, the study will target such a structure for the boron doped emitter of both IBC and iPERx cells.
The work will comprise the following tasks:

- Physical characterization of the ‘silicon/interfacial layer/polysilicon’ structure on chemically polished Czochralski PV wafers in terms of crystallinity, thickness, doping...
- Electrical characterization in terms of dark saturation current density and contact resistance of the metallized polysilicon-based structure using as reference the conventional ‘silicon/metal’ structure.

**Type of project:** Thesis with internship project

**Degree:** Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

**Responsible scientist:** For further information or for application, please contact Ivan Gordon (Ivan.Gordon@imec.be), Filip Duerinckx (Filip.Duerinckx@imec.be) and Maarten Debuquoy (Maarten.Debucquoy@imec.be).

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**Solid composite electrolyte for lithium ion battery**

Lithium ion batteries (LIB) capture about 70% of the portable electronics market and will gradually replace the nickel-metal hydride batteries in hybrid electrical vehicles (HEV). The energy and power density of existing battery technology is however not sufficient. Therefore, innovations in battery technology are badly needed and the inclination for disruptive technologies grows. Solid electrolytes are being explored to replace the flammable liquid electrolyte currently used in both inorganic and polymer Li-ion batteries. Next to resolving the issues with safety, which is imperative for automotive applications, the transition to a solid-state electrolyte would mean significant improvements in the battery performance as well: higher energy density, longer battery life time and wider temperature range of operation. Solid composite electrolytes are promising candidates. In composite electrolytes, higher Li-ion conductivities are obtained at the interface between a Lithium salt and an inert material such as alumina and silica. In our lab, we have fabricated composite electrolyte with high conductivity via sol-gel method. The properties of the electrolyte could be improved. Compatibility of the electrolyte with the electrode is to be explored. You will first optimize the sol-gel process to improve the conductivity of the electrolyte and to understand the interface interaction in the solid composite electrolyte. The compatibility issue is to be solved by tuning the properties of the solution or by modifying the electrodes. You will seek an understanding of the chemistry for the sol-gel process and learn useful electrochemical technics (e.g. cyclic voltammetry, electrochemical impedance spectroscopy) from experts. For characterization you will be introduced to analysis techniques such as FTIR, DSC, XRD, SEM, TEM, XPS, TOFSIMS as well as electrochemical techniques. For battery characterization you will need to assemble cells in inert glove box environment.
Next-generation c-Si PV modules

Photovoltaics have always been mainly (over 80%) based on c-Si solar cells, and this will continue to be the case for the foreseeable future. The module technology used for connecting and protecting these cells likewise has been established already quite some time ago and has proven its worth with operational lifetimes exceeding 20 years in harsh outdoor conditions. However, cost (and other) considerations are continuously pushing technology development towards higher performance, longer lifetimes and cheaper materials and processing. But while this pressure has in the past mostly been focused on cell development, module technology is considered to hold still additional potential for improvements.

The currently standard module technology is based on stringing of cells for electrical interconnection and subsequent EVA lamination for encapsulation of these strings between a (transparent) front- and backsheet. In this topic, the idea is to investigate the possibilities and limitations of the involved technologies, as silicone bonding, electrical interconnection and encapsulation. Afterwards, the manufactured assemblies are evaluated. With this in mind, with its extensive expertise in cell technology, imec is developing advanced module concepts. On the one hand we are developing interconnection technology for next-generation back-contact cells, implementing concepts with promising potential. On the other hand, we want to investigate the options for incorporating additional components as bypasses and switches to make modules “smarter” and able to harvest more energy from realistic outdoor conditions.

This topic is very multi-disciplinary in nature, as it looks both at the technology for PV module fabrication (with limited size), as well as the characterization and operation aspects of those modules. The focus can be adapted to some extent to the interest and capabilities of the applicant.

Electro-thermal outdoor measurements including temperature and wind effects for photovoltaic modules

Photo-voltaic solar panels provide a very attractive solution for future clean energy provision on site. Today’s panels provide a relatively high efficiency under optimal conditions and when just fabricated. However, when external temperature, radiation angle, and radiation concentration conditions are varying, also the power efficiency fluctuates quite heavily. Moreover, light intensity variation, temperature distribution and highly varying wind effects do play a significant role in the thermal processes.
The range of these effects heavily depends on the context in which these panels are used and on the type of technology used. We will mainly focus on crystalline silicon flat-plate modules using the most cost-effective solar cells.

In this thesis, we want to measure the above effects on flat-plate modules installed on a building rooftop. We will compare a number of module topologies, including several ways to introduce run-time “knob” control. We also want to measure the I-V curves where both thermal and wind effects will be included. This will contribute heavily to the energy-yield efficiency over the entire life time of the future solar system. That will result in a large practical impact of the work in this thesis.

**Type of project:** Thesis and/or internship project

**Degree:** Master in Industrial Sciences and Master in Engineering majoring in electrotechnics/electrical engineering, energy

**Responsible scientist(s):**
For further information or for application, please contact Jonathan Govaerts (Jonathan.govaerts@imec.be) and Francky Catthoor (Francky.Catthoor@imec.be).

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**Development and evaluation of illumination equipment and demonstrators for indoor PV module measurements**

It is well known that photovoltaic (PV) modules yield a lower energy in the field than what could be expected from their rated power, indicated as “peak-Watts (Wp)”. This rating is determined, according to an industrially and internationally accepted standard, under “Standard Test Conditions (STC)”. These conditions involve amongst others an irradiance of 1000 W/m² (“AM1.5 spectrum”). Knowing that these values, in climates such as Belgium’s, can only be maintained for longer periods of time on very sunny days with clear skies, it is clear that these conditions are relatively rare throughout the year and indeed the rated power effectively only indicates “peak” performance of the module.

In fact, the main energy yield losses (kWh/kWp), in particular in Belgium, can be attributed to a reduced illumination resulting in lower current and non-uniform illumination conditions (shading, clouds, soiling, ...) leading to current mismatch in the serially connected cells inside the module.

Therefore, in this topic, we want to build an illumination setup for large-area (1x1.6m²) PV modules in order to more accurately evaluate panels in conditions that are closer to reality. Concretely, we want to be able to illuminate at lower irradiance levels, that can be applied with spatial non-uniformity and that can be varied in time. Apart from building this hardware (involving optical as well as electrical considerations), the next phase is of course testing and characterizing the setup itself, and finally using the realized equipment to assess the performance of advanced PV modules we are building within the same project, coined SmartPV.

We also want to finalize a set of module demonstrators with specific topologies, intended for the same SmartPV project. Measurements with this illumination setup and the demonstrator modules will then later on (outside the scope of this topic) be used to validate some complex optical-thermal-electrical models we are building to predict and evaluate the potential energy gain of smart PV modules.

**Type of project:** Thesis and/or internship project

**Degree:** Master in Industrial Sciences and Master in Engineering majoring in electrotechnics/electrical engineering, energy

**Responsible scientist(s):**
For further information or for application, please contact Jonathan Govaerts (Jonathan.govaerts@imec.be) and Francky Catthoor (Francky.Catthoor@imec.be).
Modeling of wind effects on the energy yield of advanced and smart PV modules

Photovoltaic solar panels provide a very attractive solution for future clean energy provision on-site. Today’s panels provide a relatively high efficiency under optimal conditions and when just fabricated. However, when external temperature, radiation angle, and radiation concentration conditions are varying, also the power efficiency fluctuates quite heavily. Moreover, the variation of light intensity within the panel and highly varying wind effects do play a significant role in the thermal processes.

In order to develop the next generation Smart PV modules (integrated DC/DC converters, active by-pass switches, reconfigurable topologies etc.) more insight in thermal processes in the PV module is needed to evaluate the potential energy gain of Smart PV modules.

Indoor and outdoor experiments have shown that thermal behavior of PV modules is significantly influenced by wind effects. This master thesis focuses on investigating the effect of forced convection on the thermal response and hereby the electrical response of PV modules. Wind tunnel and outdoor setup measurements will be used to build and validate complex models which can be used to predict the thermal behavior of PV modules during any given condition. Finally, these models can then be incorporated into a complex optical-thermal-electrical model to evaluate the potential energy gain of smart PV modules.

**Type of project:** Thesis and/or internship project

**Degree:** Master in Industrial Sciences and Master in Engineering majoring in electrotechnics/electrical engineering, energy

**Responsible scientist(s):**
For further information or for application, please contact Francky Catthoor (Francky.Catthoor@imec.be) and Hans Goverde (Hans.Goverde@imec.be).

Analysis and interpretation of smart PV modules measurements

Photovoltaic (PV) solar panels provide a very attractive solution for future clean energy provision on-site. State-of-the-art, optimally installed PV modules preform excellent during clear-sky conditions. However, their energy yield reduces dramatically during non-steady state and installed at places which suffer from non-uniform illumination (e.g. static shading created by tree).

Imec is developing PV modules with additional or novel components to improve energy yield, especially during high-varying conditions and non-uniform illumination. First prove-of-concept modules are being installed and monitored to investigate the energy yield of these smart PV modules. The electrical characteristics of PV modules depend on ambient conditions like ambient temperature, irradiance, wind speed and wind direction. Due to the highly varying character of these parameters, high frequency measurements are required in order to evaluate energy yield of the smart PV modules. Furthermore, more and more conventional PV systems are monitored nowadays. Both measurement campaigns creates an enormous stream of valuable information. In order to prove the benefits of additional components, or to detect faulty PV systems, we need to analyze this information.

The student will have to collect, combine and analyze information coming from both smart PV modules, as well as information from conventional PV systems. The student has to use this analysis to identify potential gains under each specific situation. If required, the student can perform additional (indoor or outdoor) measurements. Furthermore, the student will analyze energy yield of congenital PV systems for system fault detection and to use as a reference for smart PV module.

**Type of project:** Thesis or thesis with internship project
Analysis of complex organic materials: application of G-SIMS and the G-ogram

The chemistry at surfaces and interfaces is of major importance to the correct operation of many high-innovation products including drug delivery systems, medical devices, organic electronic displays and personal care products. Secondary ion mass spectrometry (SIMS) has become a successful and popular technique to study such materials owing to its high chemical specificity, ppm surface sensitivity and the ability to image with spatial resolutions of hundreds of nanometers. More recently, the ability to molecularly image many organic materials in 3D with depth resolutions up to 5 nm has become possible. This measurement breakthrough allows complex structures such as a pixel from an organic light emitting diode to be characterized in exquisite detail. However, a complication and barrier to wider uptake of SIMS, especially for organic materials, is the complexity of the mass spectrum. To help analysts, the G-SIMS method (from gentle-SIMS) was developed to simplify the spectra and provide direct interpretation based on the physics and chemistry of the SIMS process rather than on statistical analysis techniques such as principal component analysis (PCA) or library matching methods. This has led to a family of methods with the “G” prefix [1]. The G-SIMS method has already been explored at IMEC [2] and applied successfully on organic solar cell materials. However further research is needed in order to define more precisely the application domains of this method (type of materials; achievable resolution, ....). Furthermore, when G-SIMS is applied as sole method, it is very difficult to identify multiple compounds in mixed organic materials. This is a severe limitation as most technologically relevant materials are not made from pure components. In order to circumvent this limitation and additional method called G-ogram (see short description in [1]) has been developed that allow to separate multiple components in the spectra. However, the G-ogram method has, up to now, only been described as a proof of concept. The aim of this thesis/internship is to investigate the application of this method to a variety of systems in order to achieve a better understanding of its possibilities and limitations. The work will be concentrated on organic photovoltaics materials but will also include standard polymer mixtures as references.

[1] “G-SIMS—a powerful method for simplifying and interpretation of complex secondary ion mass spectra” Ian S. Gilmore, Satoka Aoyagi, Ian W. Fletcher and Martin P. Seah; Spectroscopyeuropa, 24, 6, 2012

Type of project: Thesis or internship project

Investigation of electric potential in organic materials using Kelvin probe force microscopy

In the recent years, organic photovoltaic (OPV) cells have received much attention from the scientific as well as the industrial community, as they may offer inexpensive power generation for a wide range of applications and can for instance be integrated in packaging, clothing, flexible screens, windows, etc. They are thus an important route to introduce more renewable energy in our current society. However, continuous input from the metrology
perspective is required for the improvement in the power conversion efficiency of these solar cells as this is currently a major drawback of this type of solar cell. Therefore, nanometer scale information of active energy levels of the photo active layer is crucial to understand the process for efficient charge generation and separation. Kelvin probe force microscopy (KPFM) is a non-contact scanning probe microscopy technique to probe surface electric potential. In this work, the KPFM technique will be used to investigate the active energy levels in organic solar cell materials. This project will primarily focus on work-function characterization of polymer: fullerene solar cells. Since KPFM is a surface sensitive technique, in order to probe the energy levels deeper in the bulk of the photo active layer, the work will be focused on the cross section of these solar cells. Further, energy level alignment at the organic-metal interface will be investigated.

![KPFM images of the surface of a P3HT:PCBM solar cell](image)

**Type of project:** Thesis and/or internship project

**Degree:** Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering, energy, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Kristof Paredis (kristof.paredis@imec.be) and Thomas Hantschel (thomas.hantschel@imec.be).

**Contacting, interconnecting and packaging of thin film photovoltaic modules**

Thin film photovoltaic devices can be processed on substrates as glass, plastic film, metal foil or paper. In combination with the variability of the photoactive material, arbitrarily shaped flexible solar cells of different colors can be designed for a wide range of applications. Even semi-transparent solar cells for window integration have been demonstrated already. The organic or inorganic active materials of thin film solar cells require a stable packaging in order to protect the layers from external stress. Beside the mechanical protection, the major reason for an encapsulation is the prevention of water vapor and oxygen ingress. When reacting with the photoactive materials, both gases alter device performance and reduce the overall lifetime. At the current stage, the low device stability of organic or perovskite based solar cells is hindering printable thin film technologies from entering the market.
Within the project, different encapsulation techniques have to be developed and investigated in dependent on the target application. Flexibility or transparency are our main focus points. Another target of the work is the development of stable electrical contacts of the photovoltaic modules. For large area applications, a combination of modules requires stable electrical interconnections as well. The student is going to adapt current characterization methods according to the process and the device properties. Finally, for the selected solutions a reproducible packaging and contacting process has to be developed in the frame of this internship. The candidate should be able to independently propose and implement the technological solutions following guidelines and recommendations.

**Type of project:** Thesis and/or internship project

**Degree:** Master in Industrial Sciences and Master in Engineering majoring in materials engineering, electrotechnics/electrical engineering, energy

**Responsible scientist(s):**
For further information or for application, please contact Robert Gehlhaar (gehlhaar@imec.be).

**Air stability of perovskite photovoltaic devices**

Perovskite solar cells based on hybrid organic-inorganic lead halide-based materials recently reached 20% efficiency turning them into a candidate for future photovoltaic applications. Organic-inorganic metal halide-based materials are a broad family of components that crystalize into an AMX3 (where A is an organic ammonium cation, M is a metal atom, and X is a halide anion) structure. As a relatively new class of photoactive materials there are still many unknown properties. For instance, an air aging step is commonly reported during device fabrication but prolonged air exposure is also shown to degrade devices. The exact species and mechanisms involved are not known, but would be of benefit to create strategies for stability and performance enhancement of devices.

This project is focused on understanding the effects of oxygen and water vapor in the air stability of perovskite solar cells. During the 6-9 months internship the student is going to adapt a setup for sample measurements in a controlled atmosphere. In a first step barrier properties will be determined by a calcium test. This knowledge will be used to ascertain the effects of oxygen and water vapor on perovskite solar cells stored in different atmospheres.

We are looking for a candidate that is willing to work independently on the development of technological solutions. In collaboration with our team, the measurements are analyzed and improvements in the device fabrication and composition are proposed. The main tasks during the project will be designing parts for the measurement setup and conducting electrical and optical measurements of the devices.
Thin-film lithium-ion conductors for solid-state batteries

In the past decade lithium-ion batteries (LIB) have gained much attention in portable consumer electronics due to their high-energy density, high voltage, excellent shelf life and safety, which makes them the best choice for rechargeable batteries for devices such as mobile phones, laptop computers, tablets and energy harvesters. Although LIBs have already captured most of the portable electronic market there are still significant improvements that have to be investigated in order to improve the current state-of-the-art technology. The introduction of solid-state materials is an appealing approach which tackles the issue of intrinsic safety while at the same time boosting battery performance. Replacement of liquid electrolyte by a solid-state component allows compact packing of the cell component and thus more active material in the same volume. This would provide higher energy density as well as a potential for high power capability. The development of solid-state lithium-ion conductors with both high ionic conductivity and excellent (electro)chemical stability are needed to enable the solid-state battery technology. Thin-film microbatteries are the first generation of solid-state batteries. Here, three-dimensional microstructures are being explored for increasing the effective surface area with the aim of boosting the current density, power capability and energy storage capacity.

In this thesis work, you will be collaborating on the development of novel inorganic thin-film electrolyte materials. Both glasses (e.g. LiPON) and crystalline materials (e.g. spinel electrolytes) are under development. The experimental work will be carried out in the state-of-the-art IMEC research facilities. Thin film deposition is done in several high-tech equipment available in IMEC cleanrooms (i.e. sputtering, CVD, ALD). A number of tools are available for material characterization such as physical representation (i.e. SEM, XRD), electrical performance (i.e. cyclic voltammetry) and electrochemical behavior (i.e. impedance spectroscopy, galvanostatic charge/discharge). The main objectives of this work will be to: 1) create defect-free solid-state films with high ionic conductivity by optimizing the electrode/electrolyte/electrode compatible 3D stacks 2) quantify ionic transfer improvement with different interface configurations 3) create conformal electrodes and electrolytes in 3D thin film Li-ion batteries using effective deposition methods.

The huge challenge of this project is the creation, test and operation of inorganic Li-ion electrolyte films while still maintaining a proper mechanical integrity to increase overall lifetime performance. The student involved in this project will acquire expertise in nano-materials through applying different deposition methods for film growth and using several material characterization tools. He/she will improve his/her knowledge in physical chemistry, electrochemistry, material science and thin film technology.

Type of project: Thesis or thesis with internship project

Degree: Master in Science and Master in Engineering majoring in nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Alfonso Sepulveda (Alfonso.SepulvedaMarquez@imec.be).
Fabrication and characterization of micro-structured current collectors for 3D thin-film Li-ion batteries

The current planar (2D) thin-film Li-ion battery device has very limited storage capacity. As a result, a large areal footprint is required to provide the energy needed for the intended application. Surface structuring is proposed to increase the battery capacity for same footprint. These so-called three-dimensional (3D) thin-film batteries are much more than just a vehicle to increase capacity; it allows the electrode film thickness to be scaled down so that the battery charging kinetics can be increased drastically. However, a bottleneck in the fabrication of these 3D thin-film batteries is the 3D substrate itself. A possible route for the fabrication of these substrates, is using the self-alignment features of anodized aluminum oxide (AAO) and subsequent electrochemical deposition of (nano)-wires.

During the master thesis, different concepts using the AAO route (or similar) will be tested for creating 3D substrates for thin-film Li-ion batteries. The student will fabricate and characterize these substrates using e.g. XRD, SEM and electrochemical analysis. Different (electrochemical) fabrication methods will be investigated to create these well-defined 3D structures for their subsequent use as a substrate for the deposition of thin-film Li-ion battery materials.

The final goal is to identify a viable route for the fabrication of these 3D substrates and understanding and controlling the underlying growth mechanisms. During the thesis the student will learn about electrodeposition, related material characterization techniques and thin-film Li-ion battery theory. The master thesis student will assist in regular group meetings to present and discuss his/her data. For the candidate a background or interest in (electro)chemistry is preferred; however anyone with a background in science/engineering who is willing to learn new concepts is welcome to apply.

Type of project: Thesis or thesis with internship project

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Philippe Vereecken (Philippe.vereeken@imec.be) and Sébastien Moitzheim (sebastien.moitzheim@imec.be).

Conformal deposition of Li-ion conductors for 3D thin-film batteries

The successful adoption of lithium-ion batteries in most consumer electronic applications and a large interest in integrating them in electric vehicles drives the ongoing research and development of this type of energy storage devices. The main focus of battery research lays in material innovation, i.e. search for novel chemistries, design improvement through nanotechnology and exploration of novel electrolyte materials. This thesis project focuses on the development of solid-state electrolytes based on a thin-film platform with the emphasis on conformal material deposition and interface control. The solid Li-ion conductor or electrolyte is the most crucial part on the way to improve the battery performance and safety through all solid-state battery configuration.

The experimental work of the project is carried out at Imec facilities. Next to the fully equipped battery lab and thin-film deposition facilities, the imec state-of-the-art nanofabrication and characterization facilities will be available to carry out the research. Novel methods of conformal growth of thin inorganic-organic hybrid films using a combination of atomic layer deposition (ALD) and molecular layer deposition (MLD) techniques form the basis of the project work. Next to process optimization and physical characterization, large effort goes into the electrical and electrochemical characterization of the individual thin films and half-cell stacks (battery electrode/electrolyte). The main goal is to explore thin films as solid electrolytes for 3D thin-film lithium-ion batteries.
**Type of project:** Thesis or thesis with internship project

**Degree:** Master in Science and Master in Engineering majoring in bio-engineering, nanoscience/nanotechnology

**Responsible scientist(s):**
For further information or for application, please contact Marina Timmermans (marina.timmermans@imec.be) and Ivo Stassen (Ivo.Stassen@imec.be).

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**Electrodeposition of thin film electrodes for lithium-ion batteries**

For durable micro-storage in autonomous systems and implants, 3D thin-film Li ion batteries are leading candidates. The thin-film concept provides the means for good ionic conductance through reduction of the distance for Li-ion diffusion. Combined with the large surface area of a 3D structured surface an acceptable battery capacity is maintained.

This thesis project focuses on the electrodeposition of manganese-nickel (Mn-Ni) oxide thin film as a battery electrode candidate. After the development of the deposition process, the structural, morphological, and electrochemical properties of the electrodeposited thin films will be studied on planar substrates. Feasibility of conformal electrode material deposition for 3D battery device application will be investigated. Demonstration of electrodeposited Mn-Ni oxide thin film as a battery electrode will be done at a half-cell level.

The experimental work of the project will be carried out at Imec facilities. Next to the fully equipped battery lab and thin-film deposition facilities, the imec state-of-the-art nanofabrication and characterization facilities will be available to carry out the research.

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**Composite Li-ion conductors for solid-state lithium ion batteries**

Lithium ion batteries (LIB) capture about 70% of the portable electronics market and will gradually replace the nickel-metal hydride batteries in hybrid electrical vehicles (HEV). The energy and power density of existing battery technology is however not sufficient. Therefore, innovations in battery technology are badly needed and the inclination for disruptive technologies grows. Solid electrolytes are being explored to replace the flammable liquid electrolyte currently used in both inorganic and polymer Li-ion batteries. Next to resolving the issues with safety, which is imperative for automotive applications, the transition to a solid-state Li-ion conductor or electrolyte would mean significant improvements in the battery performance as well: higher energy density, longer battery life time and wider temperature range of operation. Solid composite electrolytes are promising candidates. In composite electrolytes, higher Li-ion conductivities are obtained at the interface between a Lithium salt and an inert material such as alumina and silica. In our lab, we have fabricated composite electrolyte with high conductivity via sol-gel method. The chemical compatibility of the electrolyte with the electrode component still needs improvement. You will first optimize the sol-gel process to improve the conductivity of the electrolyte and to understand the interface interaction in the solid composite electrolyte. The compatibility issue is to be solved by tuning the properties of the solution or by modifying the electrodes. You will seek an understanding of the chemistry for the sol-gel process and learn useful electrochemical technics (e.g. cyclic voltammetry, electrochemical impedance spectroscopy) from experts. For characterization you will be introduced to analysis techniques such as FTIR, DSC, XRD, SEM, TEM, XPS, TOFSIMS as well as electrochemical techniques. For battery characterization you will need to assemble cells in inert glove box environment.
Type of project: Thesis or thesis with internship project

Degree: Master in Science and Master in Engineering majoring in chemistry, bio-engineering

Responsible scientist(s):
For further information or for application, please contact Xubin Chen (chenxu@imec.be) and Philippe Vereecken (vereeck@imec.be).

3D interconnect-based segmented bus architecture modelling and exploration

The communication and memory organisation in internet gateways and servers are a major source of energy consumption. Future technologies will lead to higher performances but also to an increased energy bottleneck. In this thesis, we want to build an exploration framework for comparing different 3D interconnect-based options for emerging processor and memory communication architectures. The main goal will be to reduce the overall energy consumption for given application workloads executed on this communication and memory architecture. Simulations will be performed based on available measurement data to calibrate the energy and performance models.

Profile: strong interest in architecture exploration and simulation, basics of microelectronic technologies with emphasis on 3D interconnect schemes

Type of project: Thesis project of minimum 6 months (full-time, at imec Leuven)

Degree: Master in Engineering majoring in computer architecture or micro-electronics

Responsible scientist(s):
For further information or for application, please contact Eric Beyne (Eric.Beyne@imec.be) or Francky Catthoor (Francky.Catthoor@imec.be).

Fig 1: Schematic diagram of (a) all-solid state battery, (b) composite electrolyte (c) Sol-gel process
IX. Sensor Systems for Industrial Applications

There are currently no Master thesis/internship projects available in this domain.
X. Microelectronic Design

Failure analysis of soldered electronic components in shock testing

Electronics can be subjected to mechanical shocks by improper handling or during transportation. The most well-known example is dropping mobile phones on the floor. One of the largest risks when the mobile phone drops too often is that the soldered joints inside the mobile phone fracture. These solder joints make the connection between the components and the printed circuit board, and when they crack, the electrical connection is broken and the component (and most likely the mobile phone) will no longer be functional. This issue of solder joint cracking became more severe due to the change from SnPb to lead-free soldering, which is imposed by the European commission for consumer electronic applications. The new lead-free solders are stronger than the SnPb material, but are less ductile and therefore cause higher stresses when the component assembly is subjected to a mechanical shock.

A first study showed a strong influence of the chosen surface finish on the fracture type (ductile versus brittle). Further investigations need to verify the impact of temperature and different solder material compositions, as well as to check the consistency of the failure mode. Although a dominant solder failure is expected, other failure modes like solder pad cratering may occur as well. For these failures, cracking occurs underneath the solder pad, inside the board material, rather than in the solder joint itself. In order to quantify and qualify the different failure types, test samples will have to be subjected to shear and pull shock testing by aid of a mini-Charpy testing system. This system allows the differentiation between ductile and brittle failure by means of absorbed energy measurements.

The objectives for this work are:
- A technical upgrade of an Imec-made Charpy testing system (reduction of friction, improve temperature stability,...)
- Perform Charpy testing experiments for different test samples (solder and surface finish variations) and temperatures and perform a statistical analysis of the results
- Perform failure analysis by cross-sectional (LOM, SEM, EDX) inspection and investigate potential causes for the different failure mechanisms observed
- Define pre-conditioning treatments (temperature, humidity, ...) for the samples in order to study the effect of ageing on the failure mechanisms and repeat the experimental loop

Type of project: Thesis or internship project

Degree: Master in Industrial Science and Master in Science and Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Riet Labie (Riet.Labie@imec.be) and Bart Vandevelde (Bart.Vandevelde@imec.be).

Finite element modeling of thermo-compression bonding for 3D stacking

3D integration is a technology which consists in stacking together several wafers or chips in order to reduce the size and improve the performance of electronic devices. Copper-copper thermo-compression bonding can be used for forming the interconnections of three dimensional integrated circuits (3D-ICs). This process ensures the mechanical and electrical connection between ICs. Pressure and temperature are needed during the whole process.

At imec, we are working on thermo-compression bonding technology to make interconnection joints between the micro-bumps on the ICs.

During this master internship, you will be involved in the finite element modelling to simulate the process of thermo-compression bonding. The analysis of finite element results allows better understanding of this process. You will perform a parametric study of various factors that influence the final bonding quality in order to optimize the process.

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You will also collect all required material data information and, where possible, measure them yourself.

**Frame of the project**
This project makes part of the 3D program in imec where various researchers work on technology, test and modeling to stack thinned 3D-chips together. You will work in a team of specialists. You will have to present your results both to the team members but also to industrial partners.
The focus of this thesis is on finite element modeling (FEM), so a good background in FEM (thermal and mechanical simulations) is required. Where possible, the results will be compared with experimental results and used to optimize the bonding parameters.

**Type of project:** Thesis or internship project

**Degree:** Master in Industrial Science and Master in Science and Master in Engineering majoring in materials engineering, mechanical engineering

**Responsible scientist(s):**
For further information or for application, please contact Abdellah Salahouelhadj (Abdellah.Salahouelhadj@imec.be), Mario Gonzalez (mario.gonzalez@imec.be) and Teng Wang (teng.wang@imec.be).

**Analysis of thermally induced stress for 3D stacked IC during processing**

Three dimensional integration is a technology which consists in stacking together several wafers or chips in order to reduce the size and improve the performance of electronic devices. In this technology, Through Silicon Vias (TSV) and micro-bumps provide the interconnections between dies. During the processing of 3D stacks, they are subjected to temperature changes or gradients. Then, these temperature change causes thermo-mechanical stresses and deformation inside the 3D stacks, due to the mismatch in thermal expansion coefficient (CTE) and Young’s modulus between the constituent materials of the stack. Thus, the thermo-mechanical reliability of the 3D stacks is one of the major concerns.

During this master internship, you will be involved in the finite element modelling to simulate the process of stacking dies together. The analysis of finite element results allows the prediction of stress and deformation induced during stacking. You will perform a parametric study of various factors that influence the induced stress. From this analysis an analytical solution can be derived.

**Frame of the project**
This project makes part of the 3D program in imec where various researchers work on technology, test and modeling to stack 3D-chips together. You will work in a team of specialists. You will have to present your results both to the team members but also to industrial partners.
The focus of this thesis is on finite element modeling (FEM), so a good background in FEM (thermal and mechanical simulations) is required. Where possible, the results will be compared with experimental results and used to calibrate the model.

**Type of project:** Thesis or internship project

**Degree:** Master in Industrial Science and Master in Science and Master in Engineering majoring in materials engineering, mechanical engineering

**Responsible scientist(s):**
For further information or for application, please contact Abdellah Salahouelhadj (Abdellah.Salahouelhadj@imec.be), and Mario Gonzalez (mario.gonzalez@imec.be).
XI. NERF

Introduction

Imec, VIB (Flanders’ leading life science institute), and the Leuven University have set up a joint basic research initiative to unravel the neuronal circuitry of the human brain: Neuroelectronics Research Flanders (NERF). Supported by the Flemish Government, NERF looks into fundamental neuroscientific questions through collaborative, interdisciplinary research combining nanoelectronics with neurobiology. It intends to push the boundaries of science, by zooming in on the working of neurons at an unprecedented level of detail. In the long run, NERF will generate new insights in the functional mapping of the brain, as well as research methodologies and technologies for medical applications, i.e. diagnostics and treatment of disorders of the central and peripheral nervous system. The NERF labs are located at the imec premises. Read more: http://www.nerf.be/.

Studying the function of neural circuits in the mouse visual system

The main aim of the lab is to understand the fundamental principles underlying the function of neural circuits during behaviour. Towards this goal we investigate how sensory information is processed along the neural pathways that generate visually guided behaviour. To accomplish these goals, our lab uses two-photon calcium imaging, electrophysiology, optogenetics and computer based analytical methods of neural activity and animal behaviour. Using these techniques we study the activity of genetically defined neurons in response to visual stimulation and perturb components of these neural circuits to understand their function in visual information processing and visually guided behavior. Ultimately, the experiments are designed to understand the fundamental principles of sensory information processing in the brains.

The visiting students are expected to have decent background in signal processing and instrumentation. Together with the visiting student we aim to build a closed-loop system to record neural activity during specific visual tasks that allow us to investigate the processing of visual information with and without sensory feedback.

Type of project: Thesis or thesis with internship project

Degree: Master in Science and Master in Engineering majoring in physics, bio-engineering, electrotechnics/electrical engineering, computer science, biology

Responsible scientist: Karl Farrow (karl.farrow@nerf.be)

For further information or for application, please contact Karl Farrow (karl.farrow@nerf.be)